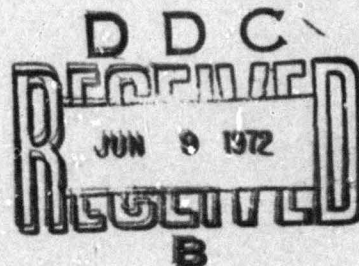RADC-TR-72-84
Final Technical Report
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HFPN IMPLEMENTATION STUDY

AVCO Corporation

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Rome Air Development Center
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13. ABSTRACT

The purpose of the investigations and hardware development described herein was to improve the reliability and performance of the coherent linear FM/CW synthesizers, delivered by AVCO under previous contracts, and based on a modification of the Hewlett-Packard direct digital synthesizer, and to demonstrate the feasibility of utilizing a new type of phase-locked VCO synthesizer for generation of the linear FM/CW waveform. The latter synthesizer was also incorporated into breadboard-type hardware to comprise a single-antenna vertical-incidence ionosonde.

Apart from minor mechanical changes, the principal improvement to the FM/CW synthesizer, based on the Hewlett-Packard equipment, was to replace the ten reference signals (3.0-3.9 MHz) previously obtained from the driver unit with an Auxiliary Driver Unit consisting of a set of crystal-controlled oscillators phase locked to a 100 kHz clock in the sweep control unit. Provision is made for fine and coarse control of the coincident zero crossing point to permit establishment of reliable coherent operation.

The phase-locked VCO-type synthesizer was selected as a possible replacement for that described above since it was determined that the close-in phase noise and spurious performance should be superior. A flexible sweep control unit was designed

14. KEY WORDS	LINK A		LINK B		LINK C	
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13. Abstract (continued)

and fabricated, with provision for positive, negative, and triangular sweep modes and a wide selection of sweep rates. Interface with the synthesizer was accomplished without difficulty and preliminary performance tests confirmed the expected characteristics.

A single-antenna vertical-incidence ionospheric sounder was assembled, consisting of the FM/CW synthesizer and breadboard models of a receiver and transmit/receive switch. Useful ionospheric soundings have been obtained at several locations.

HFPN IMPLEMENTATION STUDY

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Eldon H. Burkinshaw
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AVCO Corporation

This Final Report is submitted by AVCO Corporation, Systems Division, Wilmington, Massachusetts, under Contract F30602-70-C-0195, Job Order Number 673A0000, for Rome Air Development Center, Griffiss Air Force Base, New York. Frank Antonik (OCSL) was the RADC Project Engineer.

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A single-antenna vertical-incidence ionospheric sounder was assembled, consisting of the FM/CW synthesizer and breadboard models of a receiver and transmit/receive switch. Useful ionospheric soundings have been obtained at several locations.

EVALUATION

This report describes the investigations and hardware development performed by AVCO Corporation in the continuing phases of the 673A FM/CW development program. This effort was concerned with increasing the reliability and performance of the High Frequency Propagation Network (HFPN). At least two of the developed items have proven valuable to the network.

One item is a sweep control unit for the Dana synthesizer. This synthesizer while sweeping contained two orders of magnitude less close-in phase noise and spurious signals than the original HFPN sweepers. Two such units are now being used as the nucleus of the RADC FM/CW backscatter system. Since installation the down time due to these two units has been essentially zero.

Another item was the development of switching circuitry to alternately transmit and receive from a single antenna. Originally designed for use in a single antenna vertical ionosonde the same circuitry is being used in a single antenna repeater that is installed at Socorro, N.M. as a calibration beacon for the backscatter system. It is anticipated that more of these repeaters will be utilized in the near future, especially where the land available precludes the use of separate transmitting and receiving antennas with the necessary isolation.

FRANK ANTONIK
Project Engineer

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1.0 <u>INTRODUCTION</u>

Under previous RADC contracts, Avco has fabricated and delivered four FM/CW generators based on the modified Hewlett-Packard Model 5100 direct digital synthesizer. These synthesizers, in conjunction with various receivers and two models of the Collins auto-tune transmitter modified and interfaced by Avco, have permitted the conduct of high-resolution narrow-band and wideband ionospheric sounding in both forward scatter and backscatter modes. After some minor modifications and adjustments, the Hewlett-Packard type synthesizers have been operated in a coherent manner for narrowband operation with the ability to perform MTI and coherent integration type pre-detection processing. This performance improvement and its implications will be discussed in a forthcoming report. Despite the intrinsic advantages of direct-digital generation of the linear FM/CW waveform, resulting in the ability to perform complex analytic operations of waveform generation and pulse compression with straightforward HF receiver techniques, several practical problems arose which suggested the desirability of improvements to the original synthesizer units and an investigation of another me'...od of sweep generation based on the Dana Digiphase synthesizer which has recently been introduced.

Improvements to the Hewlett-Packard synth sizer design were primarily restricted to the Model 5110 driver unit which supplies ten reference frequencies spaced at 100 kHz intervals between 3.0-3.9 MHz and ten reference frequencies between 30-39 MHz. In order to achieve

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coherent operation of the synthesizer, the 3.0-3.9 MHz signals must be referenced to a 100 kHz clock derived from the synthesizer sweep control unit; the reference signals can be adjusted such that the zero crossings of all coincide once each 10μsec, and the coincidence point set to a specific temporal relation with respect to the 100 kHz clock. Although the original modification to the Hewlett-Packard 5110 permitted the achievement of coherent operation, the adjustment of the phase of each reference frequency was tedious, and it was found that the approach utilized was somewhat temperature dependent. Instead of attempting to further modify the driver unit, a new 3.0-3.9 MHz reference frequency source was designed and three constructed. Termed on auxiliary driver unit, it consists of ten crystal controlled oscillators, phase locked to a 100 kHz clock supplied by the sweep control unit, enclosed in a temperature-controlled cabinet. Apart from a simple fine phasing adjustment on each oscillator, the position of the coincident zero crossing point can be shifted in 0.1μsec increments with respect to the clock by a front panel thumb-wheel switch. The units have been interfaced with the synthesizers and have proved to be reliable. In addition, some minor changes and adjustments to the phase delay boards on the first FM/CW synthesizer have been made to bring the unit up to the standard of subsequent units.

A rather more substantial departure from prior art was the investigation of the suitability of the Dana Digiphase synthesizer for the generation of the linear FM/CW waveform. The instrument can be

described as a computing synthesizer in that the desired value of the phase of an ideal signal (in units of cycles and fractional cycles) is computed and compared with the actual output of a VCO whose phase is forced to agree with the computed phase by a control loop. The basic comparison interval is 10μ sec; providing that digital data in parallel BCD format is supplied at the synthesizer remote programming input during a specified time window within each 10μsec period, the frequency of the VCO can be controlled remotely and can be expected to result in a linear FM/CW ramp of exceptional linearity and purity. Conceptually, this is entirely different than the previous synthesis techniques utilized; there is no distinction between decade transitions and intra-decade transitions and, consequently, the close-in sweeping spurii of the direct digital technique are entirely absent. Sweeping spurii which do exist are at rates other than that of the desired signal and spurii at the 10μsec clock rate are completely suppressed by the characteristics of the control loop. The close-in phase noise floor is -90 db/Hz at 1 Hz offset from fo and -105 db/Hz at 50 Hz offset. This is rather better than the typical results from direct digital synthesis. In order to verify the expected performance, a compatible sweep control unit was fabricated utilizing MSI TTL logic and providing for a wide range of sweep rates, setability of frequency limits to 10 kHz resolution and positive, negative, and triangular sense modes. The resultant linear FM/CW synthesizer configuration performed as expected, exhibiting superior qualities in regard to reliability, repeatability of sweep (coherence) and phase noise floor.

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One limitation of the basic Dana synthesizer is that the principal range of the VCO is 40-51 MHz yielding only an 11 MHz bandwidth, while many ionospheric sounding applications require at least a 2-30 MHz or a 28 MHz bandwidth. In addition, it was considered desirable to provide an offset replica of the transmitted waveform for use as a receiver local oscillator. The design approach to achieving this combination of characteristics was to frequency multiply the VCO output by four, yielding a maximum sweep of 160-204 MHz, of which the range 162-190 MHz was actually utilized. This was translated to yield a principal output of 2-30 MHz and a local oscillator output of 42-70 MHz by mixing with signals of 160 and 120 MHz, respectively. Both outputs are available simultaneously. This approach does have the disadvantage of increasing the phase noise floor by 12 db at all points, but the resultant level of performance is entirely satisfactory for the intended application. In order to effect a correspondence between the sweep control unit settings and the actual output of the sweep range extender, the BCD frequency information was divided by four prior to control of the synthesizer (an undivided output is also available for application where the sweep range extender is not utilized).

The sweep control unit and sweep range extender were also utilized in conjunction with a relatively simple receiver and a solid state T/R Switch to comprise a single-antenna vertical-incidence sounder. Other hardware required for the sounder, but not deliverable under this contract,

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includes the Dana Synthesizer, broadband power amplifier (10 watt maximum), real-time audio frequency spectrum analyzer and display.

The body of the text of this report (Section 2) is organized as a discussion of the theory of operation and hardware realization of a single-antenna vertical-incidence ionospheric sounder utilizing the linear FM/CW waveform since the sweep control unit, sweep range extender, T/R Switch and receiver are deliverable equipment which have been used in this context. The auxiliary driver units and phase board modifications to the previous generation FM/CW synthesizers are discussed in Section 3. Further testing of the various FM/CW synthesizer configurations is continuing under an extension to this contract and will be reported when completed.

2.0 SINGLE-ANTENNA VERTICAL-INCIDENCE SOUNDER

2.1 INTRODUCTION

Ionospheric sounding technology has traditionally (with the exception of Appleton) utilized swept or fixed frequency pulse transmissions to measure the group delay of HF returns. About six years ago, the linear FM/CW waveform was applied to ionospheric measurements by Prof. O. G. Villard, Jr. and his students at Stanford University; shortly thereafter, our laboratory also began investigation of the technique. The linear FM/CW waveform has proved successful in all types of HF sounding, viz. oblique incidence, backscatter, RTW, and most recently, vertical-incidence sounding. In all but the latter application, the linear FM/CW waveform has the desirable property of unity duty factor coupled with an achievable range resolution limited only by the ionospheric dispersion; experimental evidence suggests that this may be considerably less than 1μ sec under ideal conditions. A corresponding disadvantage is the necessity for isolating the receiver from the transmitter to eliminate a substantial fraction of the direct (ground wave) coupled transmitter energy. The separation required depends on the transmitted power level and the relative amplitude between the ground wave (and associated phase noise spectrum) and the anticipated level of the desired return. In the case of low-power vertical-incidence sounding, antennas oriented orthogonally and spaced by 1,000 feet are adequate.

Many applications for vertical-incidence sounding systems mitigate against the use of two antennas separated even by 1,000 feet. The desire for portability, use of existing antennas, or airborne use precludes the implementation of a practical system if it utilizes two antennas. Consequently, another method of isolating the transmitter and receiver must be sought. The most obvious, and the one, in fact, selected is to pulse the linear FM/CW waveform in a manner which might, at first, appear similar to a conventional sounder, but is, in reality, quite a departure from a pulsed-cw system. The advantage gained is that the typical duty factor is approximately 0.7 and that the signal processing is similar to unity duty factor FM/CW.

2.2 CONCEPTUAL APPROACH

Figure 2.1a is the basis for understanding single antenna sounding. The discussion is given as if the transmitter output frequency and receiver l. o. were the same, resulting in homodyne detection, whereas the actual system offsets the receiver l. o. by the nominal first IF frequency. For illustrative purposes, we have assumed that the FM/CW generator is sweeping in the positive sense at a sweep rate df/dt and the transmitter and receiver are gated on alternately every 2 msec. During the entire sequence, the FM/CW generator continues to sweep, with the generator output utilized alternately as the transmitted signal and receiver l. o. during the transmit and receive periods respectively; the antenna is transferred between the transmitter output and the receiver input in accordance with the mode.
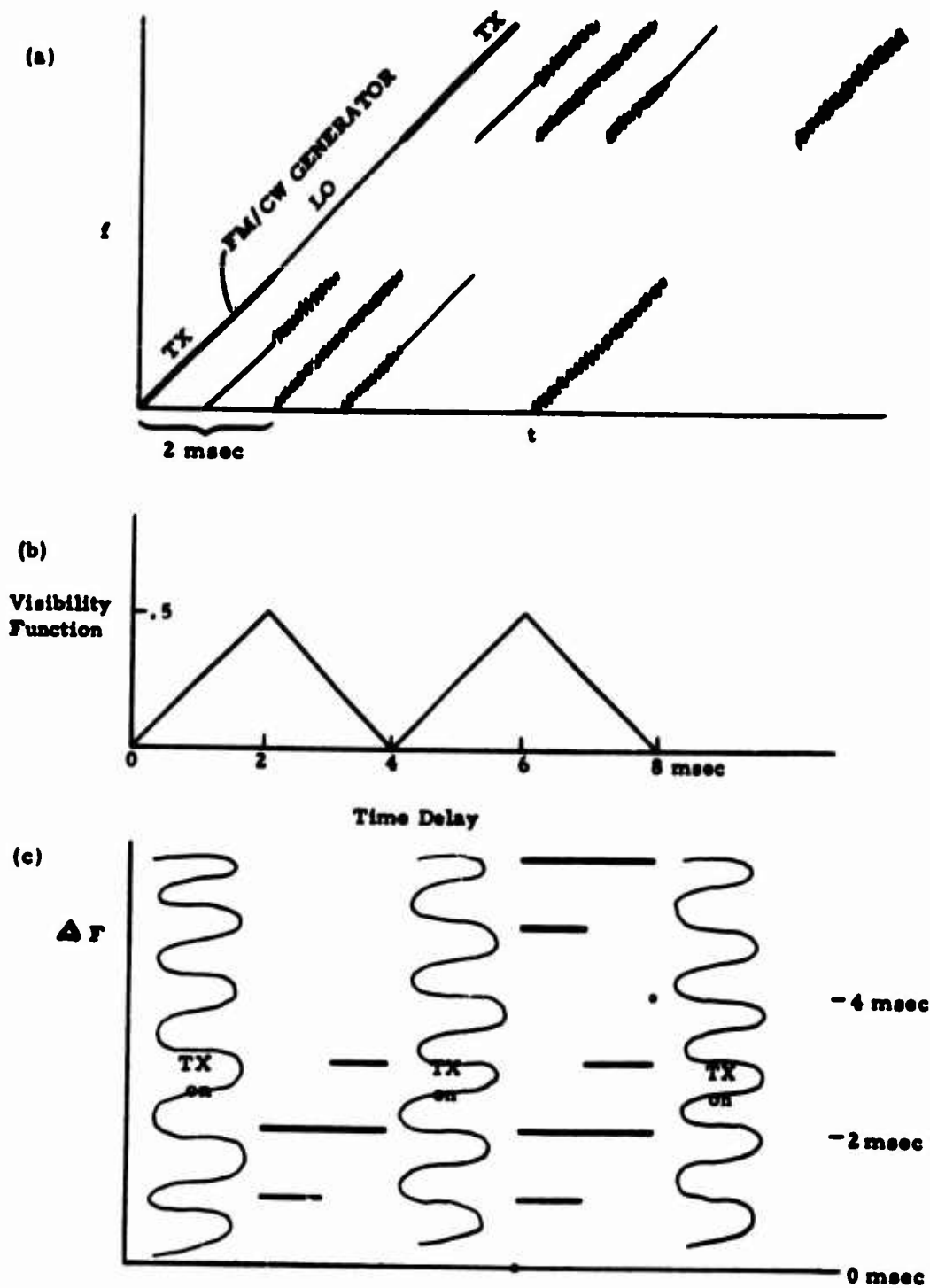
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(a)

(b) Visibility Function

Time Delay

(c)

FIGURE 2. 1

Shown also are returns from reflections at 1, 2, and 3 msec range, which are delayed replicas of the transmitted pulse. Note that the return at the closer range begins to arrive prior to the commencement of the receive interval and a portion of the return is lost, while a return from 2 msec entirely fills the receiver on gate; at greater ranges, the trailing portion of the return is lost, until finally for a delay of 4 msec the return is contained entirely within the subsequent transmit interval and cannot be received. The portion of each return which can be observed by the receiver is indicated by the wavy line. The effect of commutating the FM/CW waveform is, therefore, to impose a range visibility function on the data, which is sketched in Figure 2.1b, revealing the presence of a zero response at 0, 4, 8...msec, which is obviously undesirable since desired data may lie in the vicinity of 4 msec. We shall discuss, in a moment, how this problem can be overcome. Before treating that topic, consider the effect of homodyne detecting the received signal by mixing it with the FM/CW generator. In the case of a unity duty factor waveform, the difference frequency would be given by

$$\Delta F = -\frac{df}{dt}\tau \tag{1}$$

where ΔF = difference frequency in Hz

$\frac{df}{dt}$ = sweep rate in kHz/sec

τ = time delay in msec

When the waveform is commutated as described above, the same difference frequency relation obtains, but the energy at each frequency occurs in bursts, related to the visibility function. This effect is shown schematically in Figure 2.1c, where the magnitude of the difference frequency is plotted as a function of time for several pulses. If the spectrum analyzer employed to process the data has a typical frequency resolution of 0.5 Hz, 2 seconds of data is accumulated for analysis purposes, representing 500 pulses of the type shown. This results in recovery of the nominal frequency of each component plus the addition of sidebands related to the chopping rate. Provided that the chopping rate and sweep rate are suitably scaled, the sidebands will fall outside the data analysis bandwidth.

In order to proceed further, with the analysis of the system, some of the parameters of the real-time spectrum analyzer need to be specified. A typical analysis bandwidth would be 200 Hz with 400 frequency resolution cells (0.5 Hz bandwidth). Since the readout rate of the analyzer is of the order of 200 msec, the spectrum analysis is redundant by a factor of 10, and is utilized primarily to achieve a suitable display. Table 2.1 summarizes the range gate, T_{max}, 3 db range resolution, T_{3db}, and the time to sweep a 1 MHz frequency band. From this set of parameters one must optimize performance based on some set of criteria. For purposes of establishing such criteria, we chose to specify that the system should have a range resolution of 10μ sec since it is normally desired to scale critical frequencies to 100 kHz accuracy; this results in selecting 50 kHz/sec

as the optimum sweep rate (N. B. if other than flat weighting is desired

in the spectrum analysis process, a slightly higher sweep rate will be more

effective). Faster sweep rates may be utilized if the spectrum analyzer

bandwidth is set at 500 Hz and a higher chopping frequency selected.

TABLE 2.1

df/dt (kHz/sec)	τ_{max}(msec)*	τ_{3db}(μmsec)**	T/MHz(sec)
20	10. 0	25	50
30	6. 66	16. 66	33. 3
40	5. 0	12. 5	25
50	4. 0·	10. 0	20
60	3. 33	8. 3	16. 6
70	2. 85	7. 1	14. 3
80	2. 5	6. 25	12. 5
90	2. 22	5. 5	11. 1
100	2. 0	5. 0	10

Returning to the question of the visibility function again, we note

that the zero visibility points are related to the sum of the duration of

the transmit and receive periods; i. e. , to the pulse repetition frequency.

Consequently, the position of the zero may be adjusted by varying the

prf. This is in fact what is done, and in a manner such that the visibility

function is optimized over the range gate of interest. Let us look at a

practical example shown in Figure 2. 2. Traces 1 and 2 are the transmitter

and receiver states for the high prf and traces 3 and 4 for the low prf,

respectively. A guard band is provided between transmitter turn off and

receiver on to permit the decay of any circulating pulses in the antenna

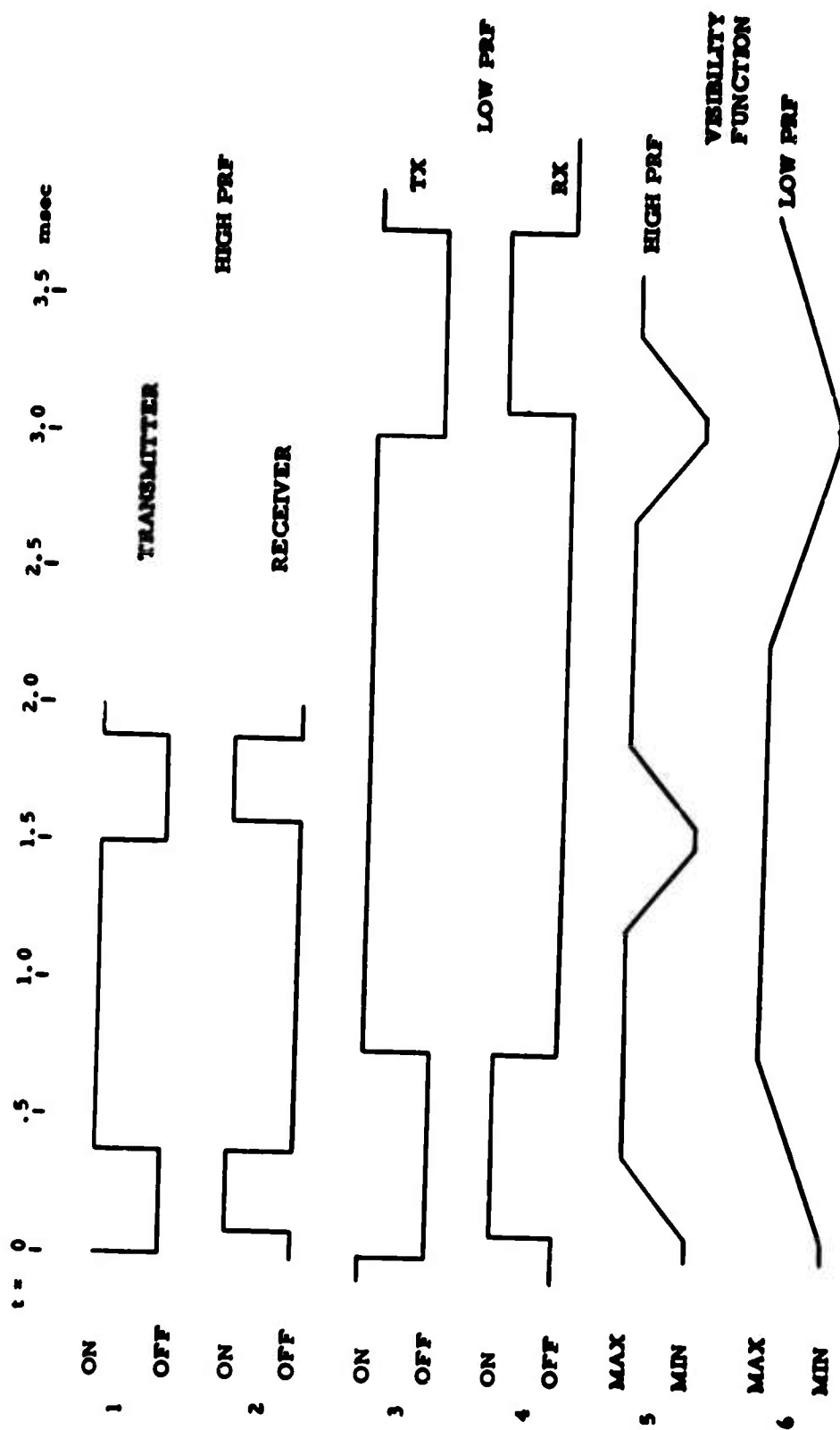*200 Hz spectrum analysis bandwidth

**400 spectral resolution cells

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FIGURE 2.2
RELATION BETWEEN PRF AND RANGE VISIBILITY FUNCTION
Refer to Appendix A

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transmission line. The corresponding visibility functions for the high

and low prf states are given by traces 5 and 6 respectively. The trans-

mitter duty factor has been increased to greater than 50 percent, yielding

a flat-top function at a slight increase in the effective receiver noise

figure. In practice, there are a total of 10 distinct prf states, only the

maximum and minimum prf being shown here. Once complete sequence

of prf states is accomplished during the time necessary to sweep over a

100 kHz band resulting in a relatively uniform visibility function consis-

tent with obtaining a range resolution of 10μ sec.

2.3 HARDWARE REALIZATION

The implementation of the concept is outlined in Figure 2.3. In

practice, the receiver has a first IF which is substantially offset from

zero (viz. 40 MHz). A FM/CW generator based on remote control of a

Dana Laboratories 7010 Digiphase frequency synthesizer by a sweep

control provides simultaneous outputs of 2-30 MHz and 42-70 MHz which

are utilized as the transmitted signal source and receiver local oscillator

respectively. They are alternately supplied to the transmitter, which is a

ten watt broadband transistor amplifier and to the receiver first mixer.

The prf control is synchronized with the sweep rate and sequences the low

level rf switches and high power T/R switch to achieve a timing plan

similar to that shown in Figure 2.2. The receiver, sweep control unit and

TR switch are deliverable breadboard items under this contract and are

described in this section. The Dana 7010 synthesizer and ENI 10 watt
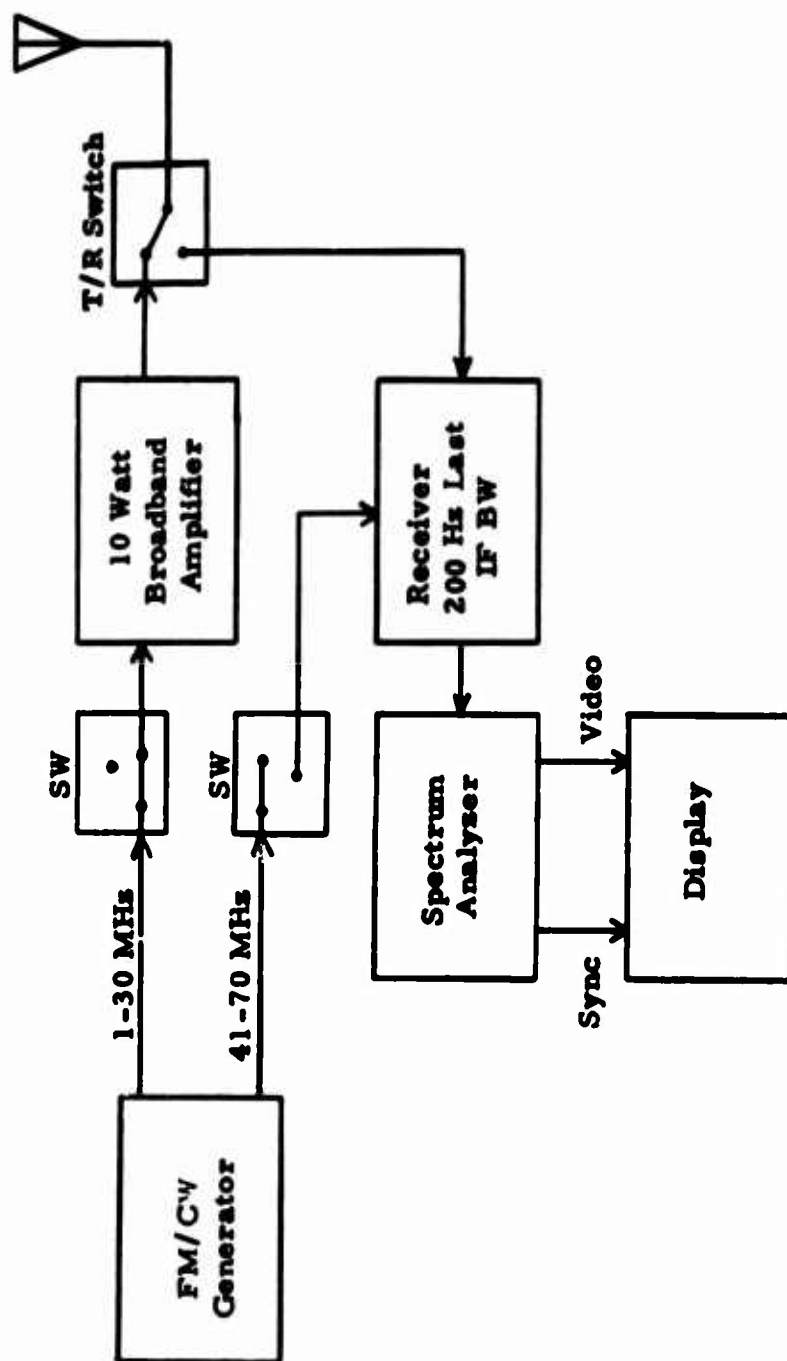
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FIGURE 2. 3

FUNCTIONAL BLOCK DIAGRAM OF SINGLE-ANTENNA
VERTICAL-INCIDENCE FM/CW IONOSONDE

amplifier are Avco property, while the spectrum analyzer and display are availab's at the RADC field sites.

The receiver is a double conversion superheterodyne output translated to baseband in a coherent (undetected) manner, and with all conversion frequencies phase locked to the synthesizer frequency standard. Manual or AGC modes are provided. The last IF bandwidth is limited to 200 Hz by a crystal filter to permit the AGC to operate and to reduce fold over of interfering signals. Spectrum analysis is performed by a real-time audio spectrum analyzer and the resultant signal displayed as z-axis modulation on a facsimile recorder.

Typical equipment operating characteristics when configured as a vertical-incidence sounder are shown in Table 2.2.

TABLE 2.2

TYPICAL FM/CW OPERATING PARAMETERS
(Vertical Incidence)

Frequency Range:	2-30 MHz (100 kHz minimum bandwidth)
Power Output:	8 watts peak, 6 watts average
Sweep Rate:	50 kHz/sec
Range Gate:	0-4 msec (0-600 km)
Range Resolution:	10μ sec
Sweep Time:	20 sec/MHz

Figure 2.4 is a photograph, sans spectrum analyzer and display of a system similar to that described in the text. From top to bottom are the Sweep Control, Dana 7010 Synthesizer, receiver and prf control, T/R Switch and 10 watt broadband amplifier.
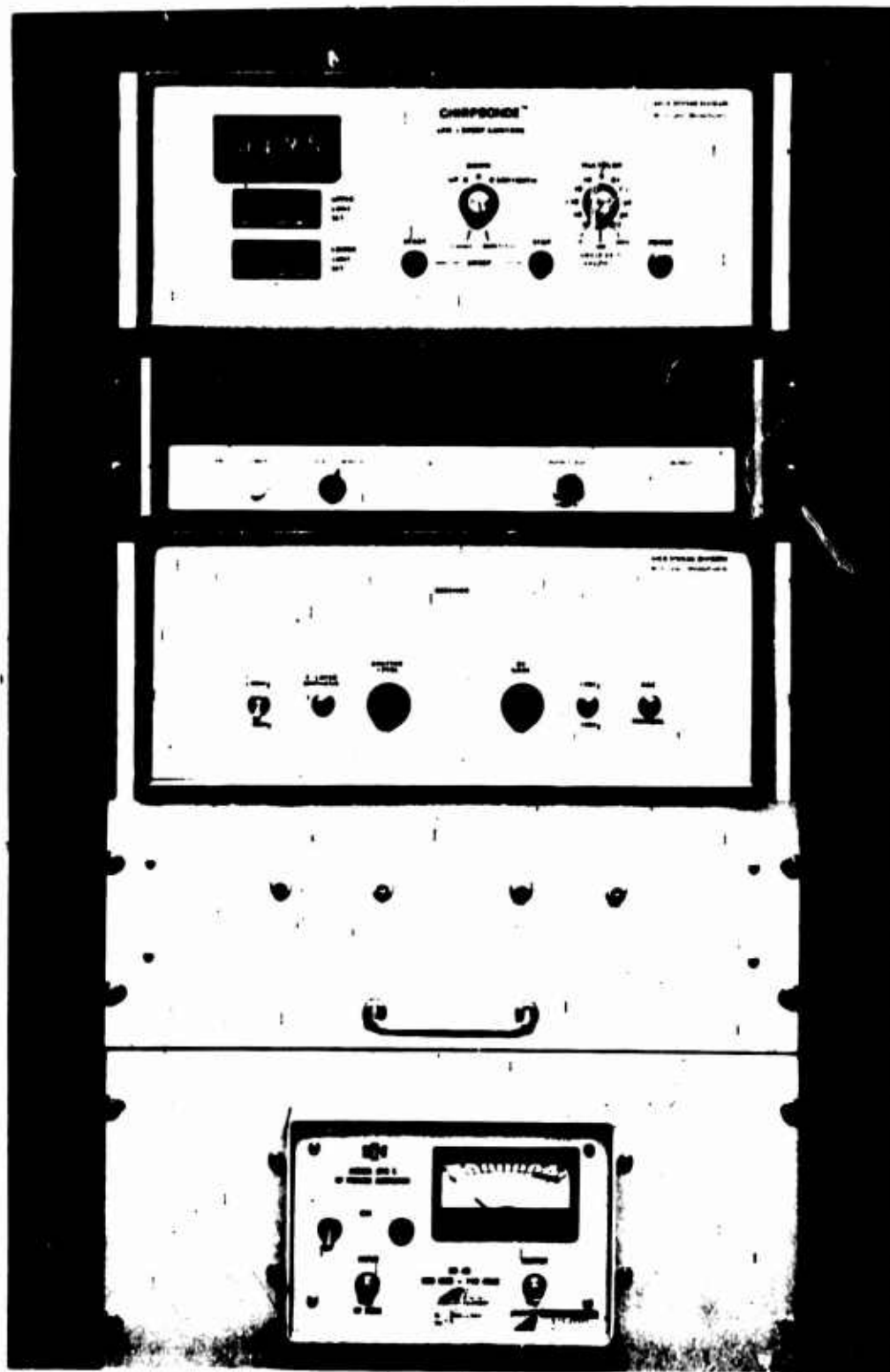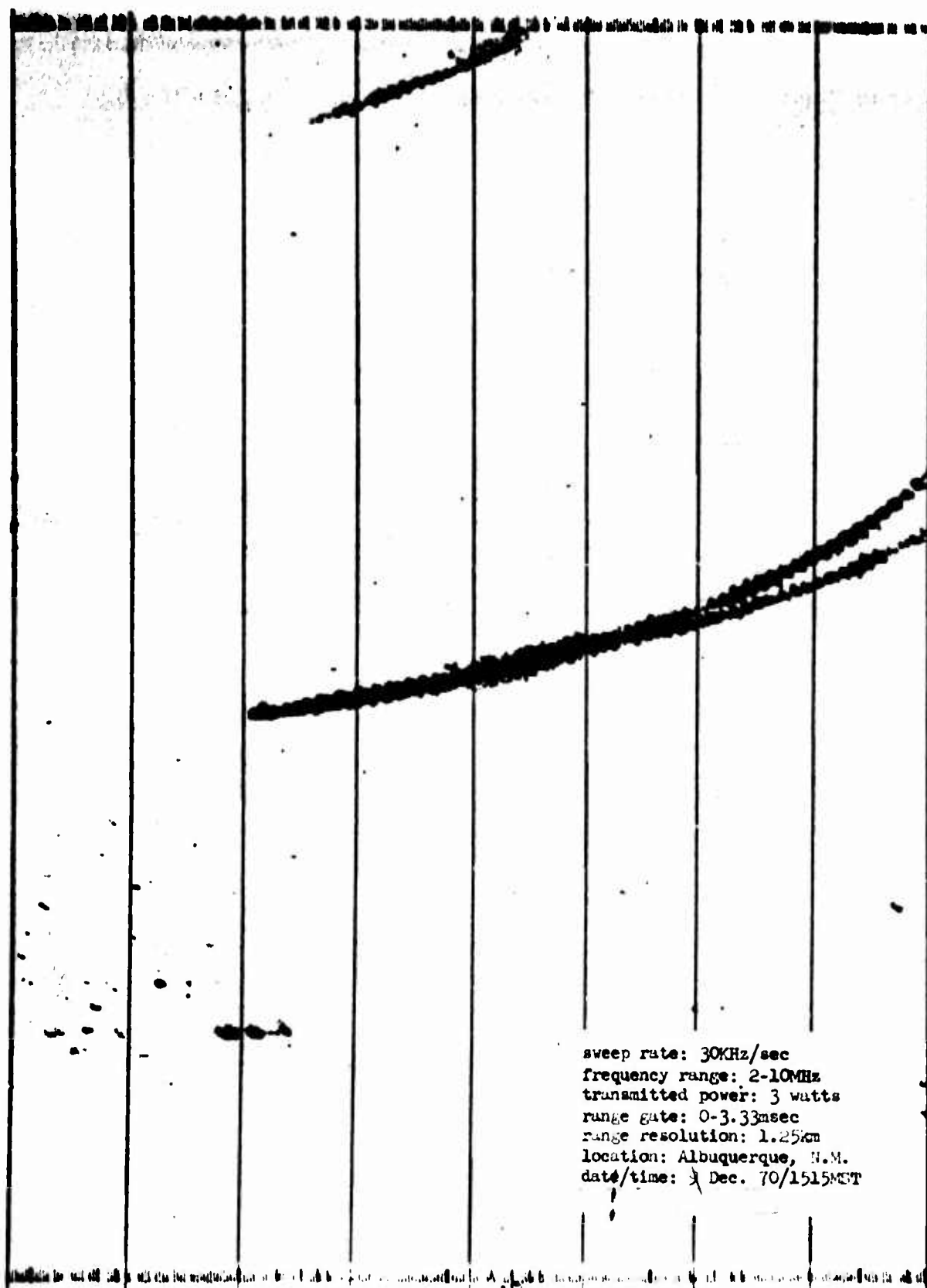
FIGURE 2. 4

sweep rate: 30KHz/sec
frequency range: 2-10MHz
transmitted power: 3 watts
range gate: 0-3.33msec
range resolution: 1.25km
location: Albuquerque, N.M.
date/time: 3 Dec. 70/1515MST

FIGURE 2.5

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An example of data obtained during preliminary system testing is given in Figure 2.5, where the sweep rate is 30 kHz/sec and a 100 Hz bandwidth analysis range was utilized, approximately equivalent in range resolution to that previously discussed. The sweep bandwidth was 2-10 MHz with approximately 3 watts forward power (measured with a thru-line wattmeter). The antenna was quite poor, as it was intended to simulate one aboard an aircraft. Frequency markers appear every MHz; the total range gate displayed is 3.33 msec (500 km).

A more detailed block diagram of the equipment when configured as a vertical incidence sounder is shown in Figure 2.6. The receiver, which is a double conversion superheterodyne has a nominal first IF of 40 MHz, second at 455 kHz and coherent baseband output. Both long time constant AGC and MGC are provided. The receiver and sweep range extender are contained in the same cabinet. The function of the sweep range extender is to produce two simultaneous output signals which can be swept between 2-30 MHz and 42-70 MHz from the Dana synthesizer output which has an overall frequency range of 40-51 MHz. As can be seen from the block diagram, this result is achieved by multiplying the synthesizer output frequency by four and frequency translation. The sweep control unit provides for setting the sweep limits, sense and rate and provides BCD logic control signals in compatible form to the Dana synthesizer, which result in a correspondence between the dial settings and the rf output; in addition, control of the prf rate is derived from an
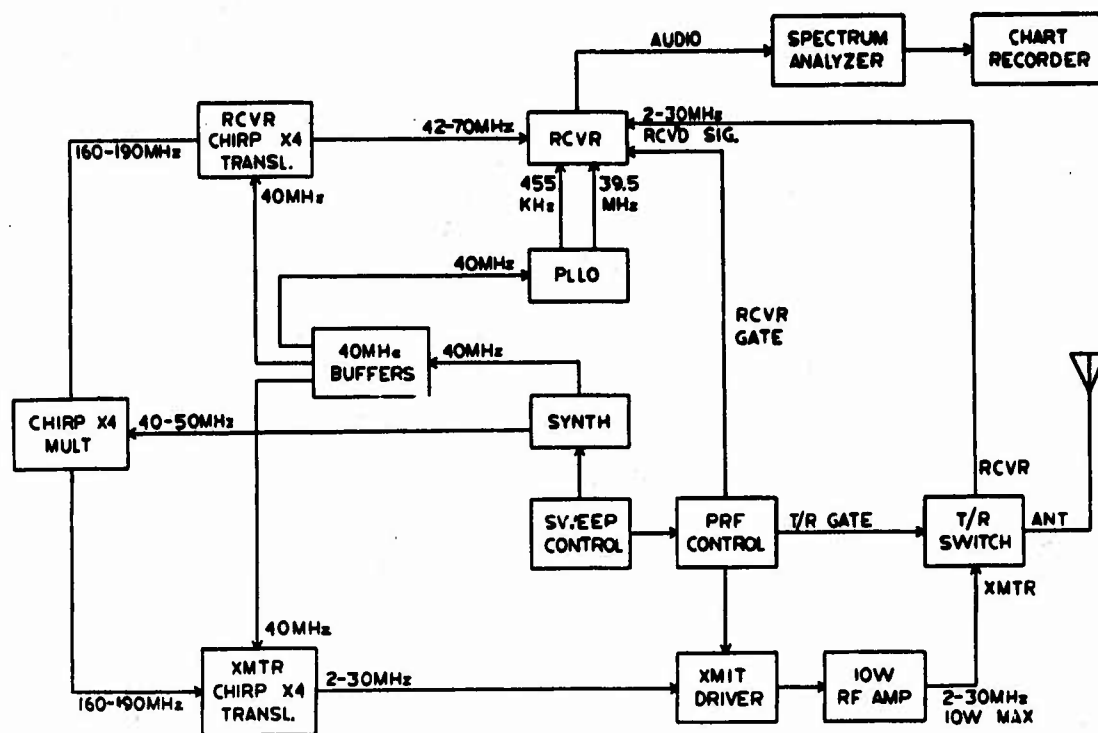
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FIGURE 2. 6   Vertical Incidence Sounder I System Block

internal counter. After amplification to the 10 watt level in a commercial solid state amplifier (not supplied under this contract) the signal is passed through the T/R Switch, which commutates the antenna between the transmitter output and receiver input, as previously described.

The following sections provide a more detailed description of the equipment deliverable under this contract, viz., breadboard models of a sweep control, T/R Switch, sweep range extender and receiver.

2.4 SWEEP CONTROL ASSEMBLY

2.4.1 Brief Circuit Description

The Sweep Control Assembly is an auxiliary to the Dana 7010 Frequency Synthesizer. The Assembly provides digital information for tuning the synthesizer. Every 10μ s the synthesizer can accept a frequency update so that if the data changes in a "staircase" fashion every 10μ s, the synthesizer output would be a frequency ramp.

The following controls have been provided:

a) SWEEP Rate Switch with positions 10 kHz/sec, 100 kHz/sec, and 1 MHz/sec

b) SWEEP RATE MULT. Switch with positions 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 and 2.5.

c) SWEEP SENSE Switch with positions UP, DOWN, and TRIANGULAR

d) SWEEP MODE Switch with positions SINGLE and REPETITIVE

e) POWER Switch

f) SWEEP START momentary action switch

g) SWEEP STOP momentary action switch

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There are also two sets of four thumbwheel switches that determine the sweep limits. They are the UPPER SWEEP LIMIT and the LOWER SWEEP LIMIT, each controlling the decades from 10 MHz to 10 kHz. The synthesizer cannot be controlled by the Sweep Control Assembly unless the synthesizer's LOCAL/REMOTE Switch is in REMOTE. In REMOTE, the Assembly obtains a + 5 volt level from the synthesizer which activates a MC1461 regulator which provides + 5 volts (Vcc) to all the Assembly logic. Since the Burroughs decoder and Nixie driver circuits use the same Vcc, the Nixie display will not energize without the Dana Synthesizer LOCAL/REMOTE Switch in REMOTE. Figures 2.7 through 2.12 are partial block, simplified, and/or logic diagrams of the Assembly, each showing some phase of the Assembly's operation.

2.4.2 Sweep Limit Control Circuitry

Figure 2.7 is a simplified diagram showing how the SWEEP UP MODE is accomplished. The following circuit description will, therefore, be developed around the SWEEP UP MODE.

A Sweep may be started by pressing the SWEEP START button which flips "on" the Count Enable Flip Flop and the Preset Flip Flop. The "preset on" is and-gated with Clock Pulse No. 3 to produce the "load signal." This signal loads the lower sweep limit into a set of eight up/down decade counters that represent the eight digits being controlled.
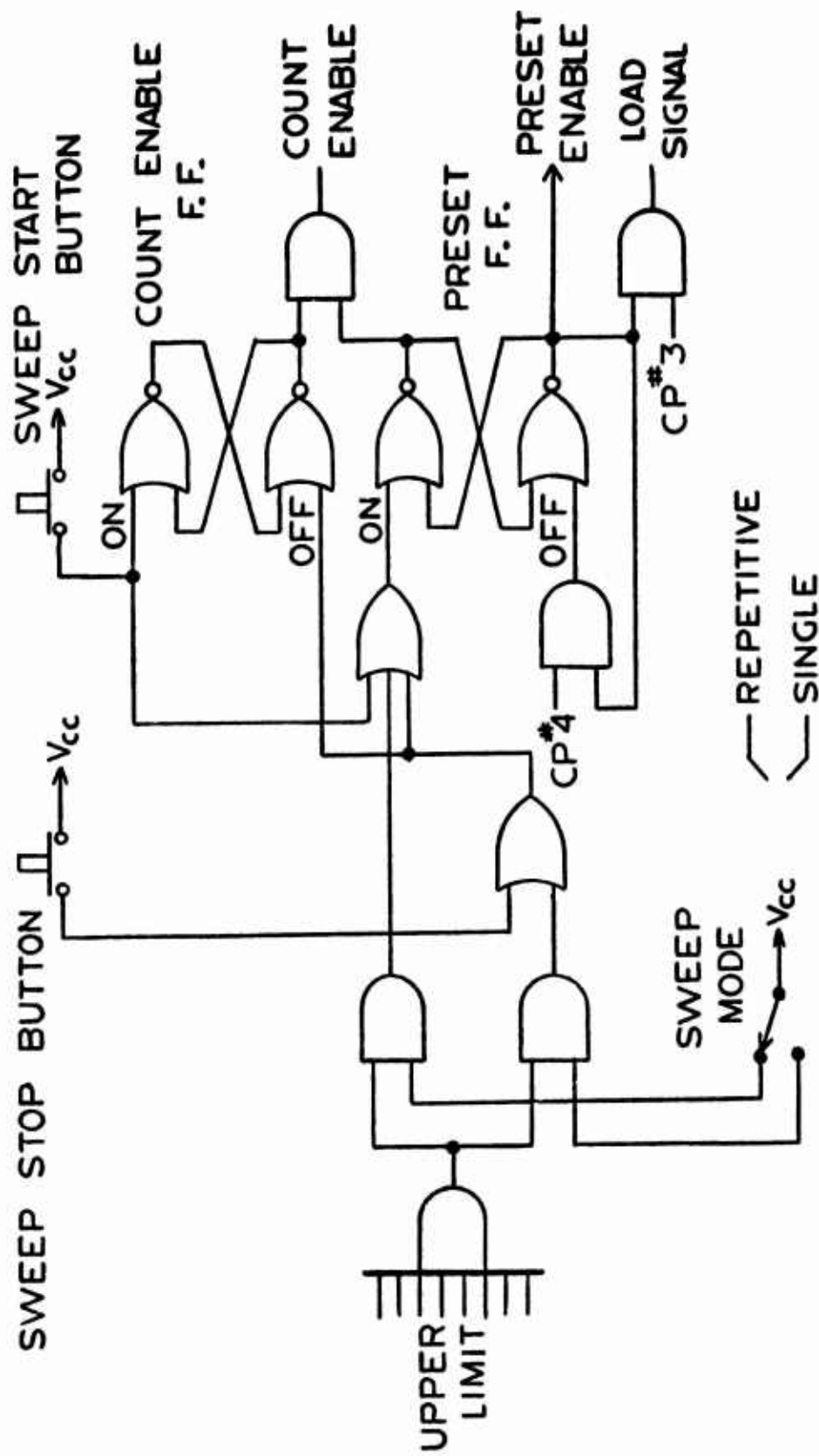
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FIGURE 2.7 Sweep Limit Control Circuitry

Clock Pulse No. 4 turns the Preset Flip Flop "off". The off side of this flip flop is and-gated with the "on" side of the Count Enable Flip Flop to produce the Count Enable signal.

If the SWEEP MODE switch is in REPETITIVE when the Upper Sweep Limit is reached, a "one" level is produced on the Upper Limit eight input gate (8 decades). This level is passed on to the Preset Flip Flop, generating another load cycle.

In SINGLE SWEEP the Upper Limit Level hits both the "on" side of the Preset Flip Flop and the "off" side of the Count Enable Flip Flop. Thus at the end of the sweep, the counter is loaded with the lower limit and the count input is stopped.

2.4.3 Burst Count Control

Since the data update window for controlling the synthesizer frequency is limited to 8 microseconds out of the 10 microsecond update interval, a minimum burst rate of 2 mpps is needed to achieve the maximum required sweep rate. Figures 2.8 and 2.9 together block out the burst count circuitry.

The 100 kHz squarewave leading edge from the synthesizer is used to mark the start of the window. It resets the divide-by-five count down and flips "on" the Burst Count Enable Flip Flop. This flip flop output is and-gated with the Count Enable level from Figure 2.7 and CP #3. In Figure 2.8, the Burst Counter, which has been reset by the Burst Reset pulse, accumulates counts until the count matches the SWEEP RATE MULT
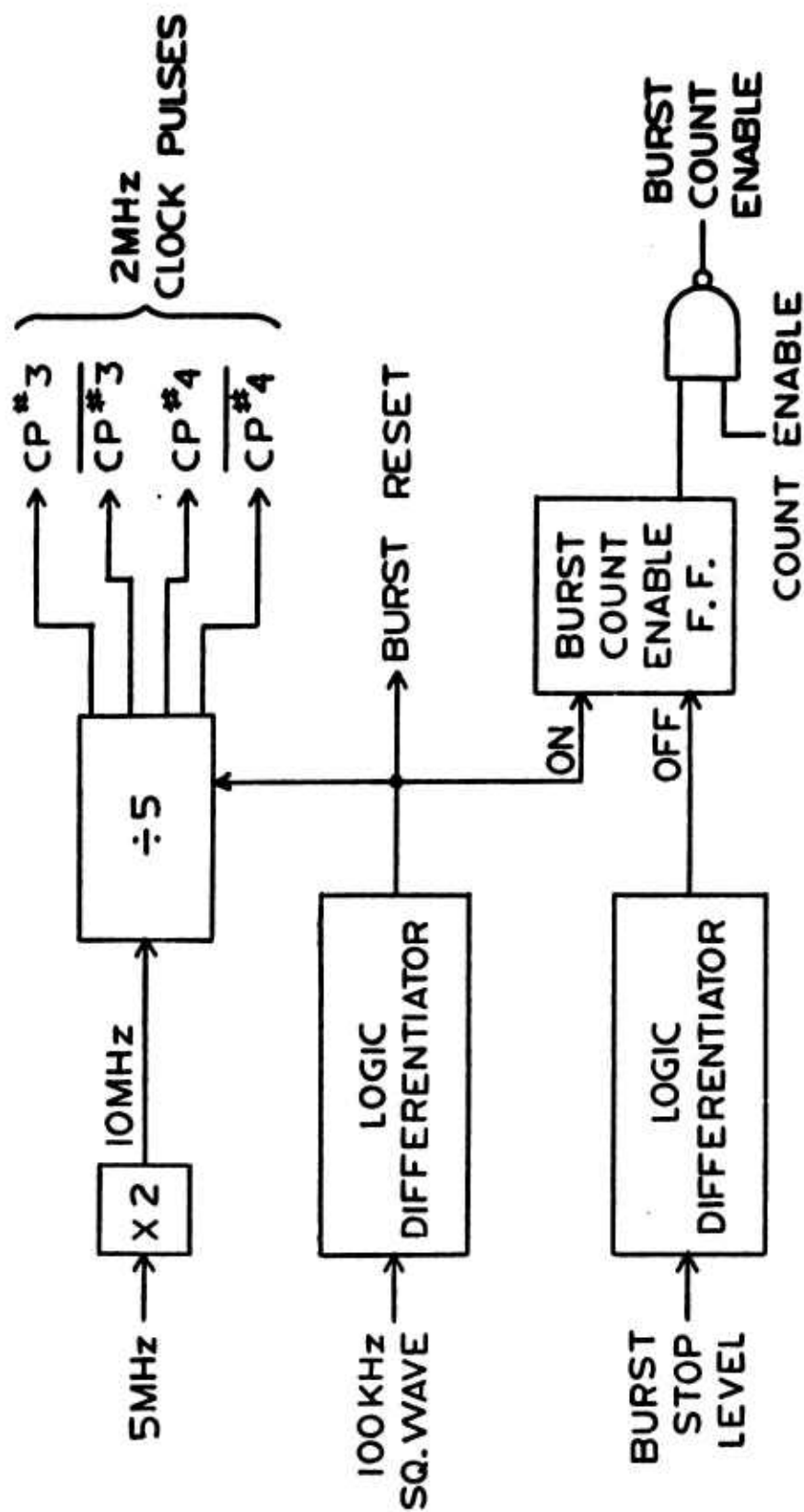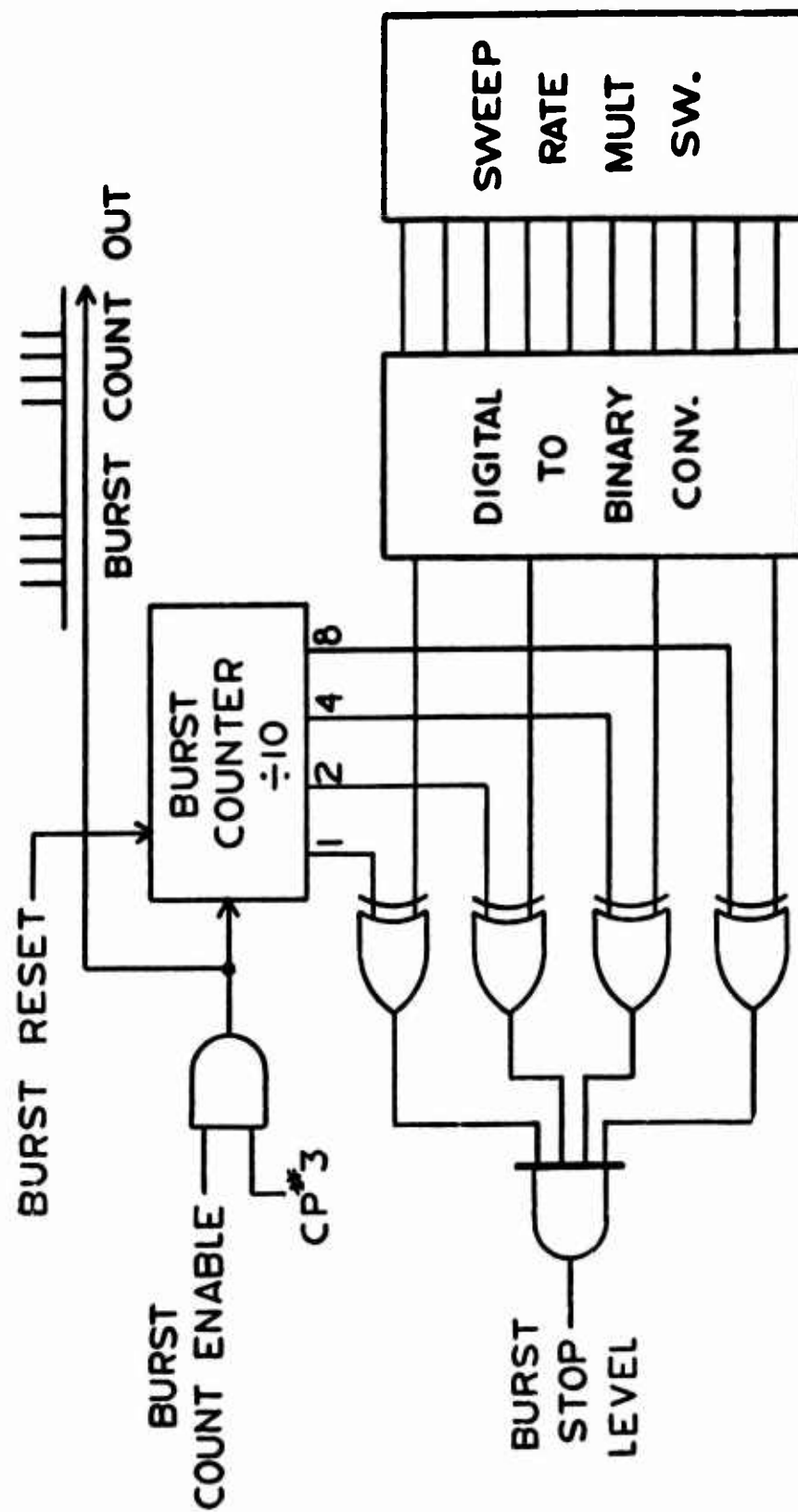
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FIGURE 2.8 Burst Count Clocking Circuitry

FIGURE 2.9 Burst Length Control Circuitry

Switch position, at which point a Burst Stop Level is generated. This level, differentiated, shuts off the Burst Count Flip Flop. The cycle begins again with the next Burst Reset pulse.

2.4.4. The Up/Down Counting Chain

The Burst Count Out is fed to the counting chain via the Sweep Control Circuitry seen in Figure 2.10. At the 1 MHz/sec rate, the burst is fed directly to the input of the 10^1 decade. At 100 Hz/sec, the input is into the 10^0 decade. And at 10 kHz/sec, the Burst Count passes through an additional divide-by-ten counter before being fed to the 10^0 decade.

As implied in Figure 2.11 all decade counters from 10^0 to 10^7 are of the Up/Down type with carry, borrow, up/down and load input connections and BCD outputs. With the up/down level at the up or "one" level, carry pulses are passed from decades left to right. With the up/down level at the down or "zero" level, borrow pulses are passed from decades right to left.

Since the first decades are not controlled by thumbwheel limit switches, the zero count for each is and-gated at the BCD output from the 10^0 to the 10^3 decades for the Upper Limit intercept determination. The BCD load inputs are wired to the zero count in order to "load in" zeros.

BCD outputs of the 10^4 to 10^7 decades are compared to their corresponding UPPER SWEEP LIMIT thumbwheel switches and and-gated. Together these outputs are and-gated by the UPPER LIMIT GATE shown
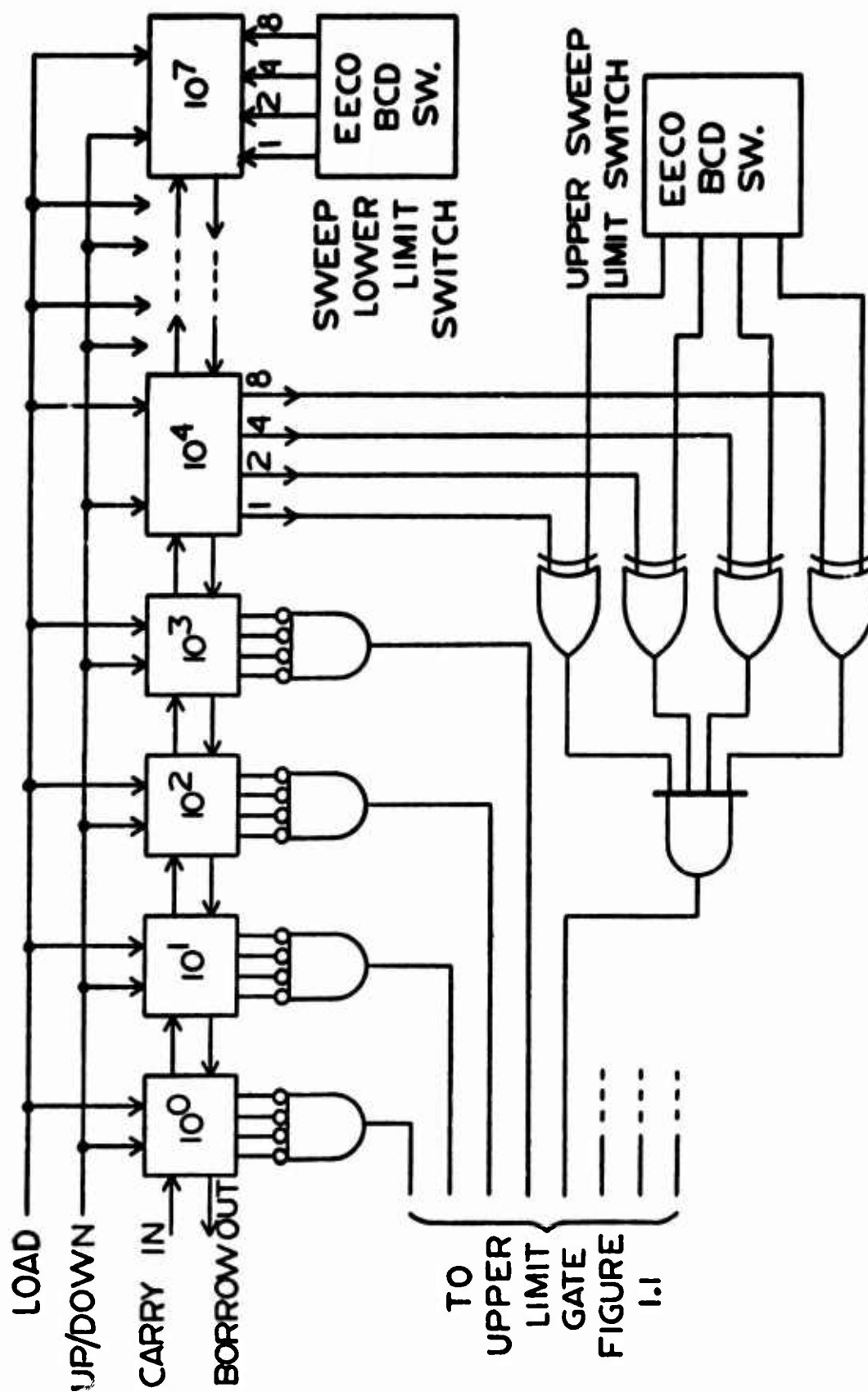
-26-

FIGURE 2.10 Basic Sweep Rate Control

FIGURE 2.11 The Up/Down Counting Chain

in Figure 2.7 to produce an Upper Limit Level which ultimately generates a load level. The count comparator circuit shown on the BCD outputs of the 10^4 decade is typical to the 10^5, 10^6, and 10^7 decades as well. Similarly, the load inputs loading in the LOWER SWEEP LIMIT on the 10^7 decade are typical to the 10^4, 10^5, and 10^6 decades. The load level simply loads in these levels at the load inputs.

2.4.5 Down and Sawtooth Sweep Modes

The sweep sense is controlled by the Up/Down Flip Flop seen in Figure 2.12. The SWEEP SENSE Switch holds this flip flop in the up mode in the UP position and the down mode in the DOWN position. In the SAWTOOTH position the Upper Limit and Lower Limit Gates trip the Up/Down Flip Flop back and forth. In this mode, a load signal is generated only once--at the beginning of the first up ramp, the start of the sequence. The last four decade counters (10^4 to 10^7) are wired identically. Note that the two SN7451's that feed the Load Inputs of each counter. Each half serves as a commutator between equivalent bits of the UPPER SWEEP LIMIT and the LOWER SWEEP LIMIT thumbwheel switches. The Lower Start Limit and the Upper Start Limit outputs shown in Figure 2.12.

2.4.6 Divide-by-Four Logic

In order to expand the frequency range of the Dana 7010 (0-11 MHz out) to cover the HF band, an analog frequency quadrupling multiplier is used to provide a potential 0-44 MHz capability. So that the Basic Sweep
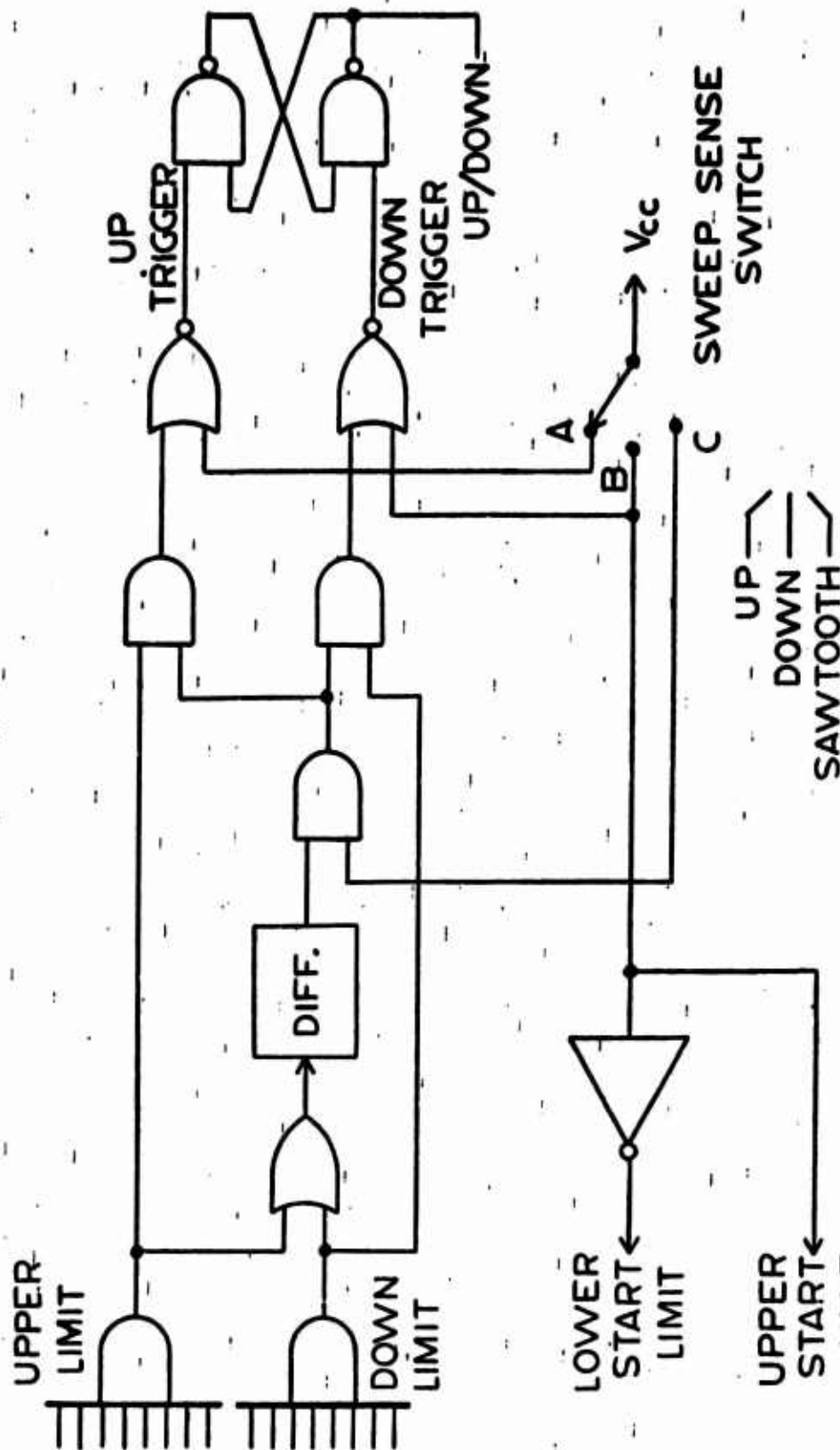
-29-

FIGURE 2.12 Up/Down Control

Control settings agree with the frequency multiplied output, the logic control output to the Dana is intercepted by logic divide-by-four circuitry. Two identical receptacles are provided on the back of the Sweep Control Assembly for the Dana interface; J1 provides the divide-by-four output and the J2 provides the direct output(see Figure 2. 13).

Developing the logic equations that this circuitry is based on is beyond the scope of this report. However, trouble shooting the divide-by-four is straight-forward since the malfunctioning decade is easily detected and each decade only involves four integrated circuits at the most.

Basic trouble-shooting procedures for this equipment are provided in operating and maintenance manual which has previously been submitted to RADC.

2.5 SWEEP RANGE EXTENDER

2.5.1 Brief Circuit Description

The Sweep Range Extender Assembly is intended to increase the frequency range of the Dana 7010 Frequency Synthesizer to 30 MHz. It accepts the 40-50 MHz and 40 MHz outputs from the synthesizer and by mixing and multiplication schemes generates a 42-70 MHz output for use as the receiver l. o. and a 2-30 MHz output for use as the transmitted signal. There are no external operator controls; the entire assembly is housed in two 9 x 6 inch aluminum boxes: one contains the wide band X4 frequency multiplier, and the other houses the two frequency translators.
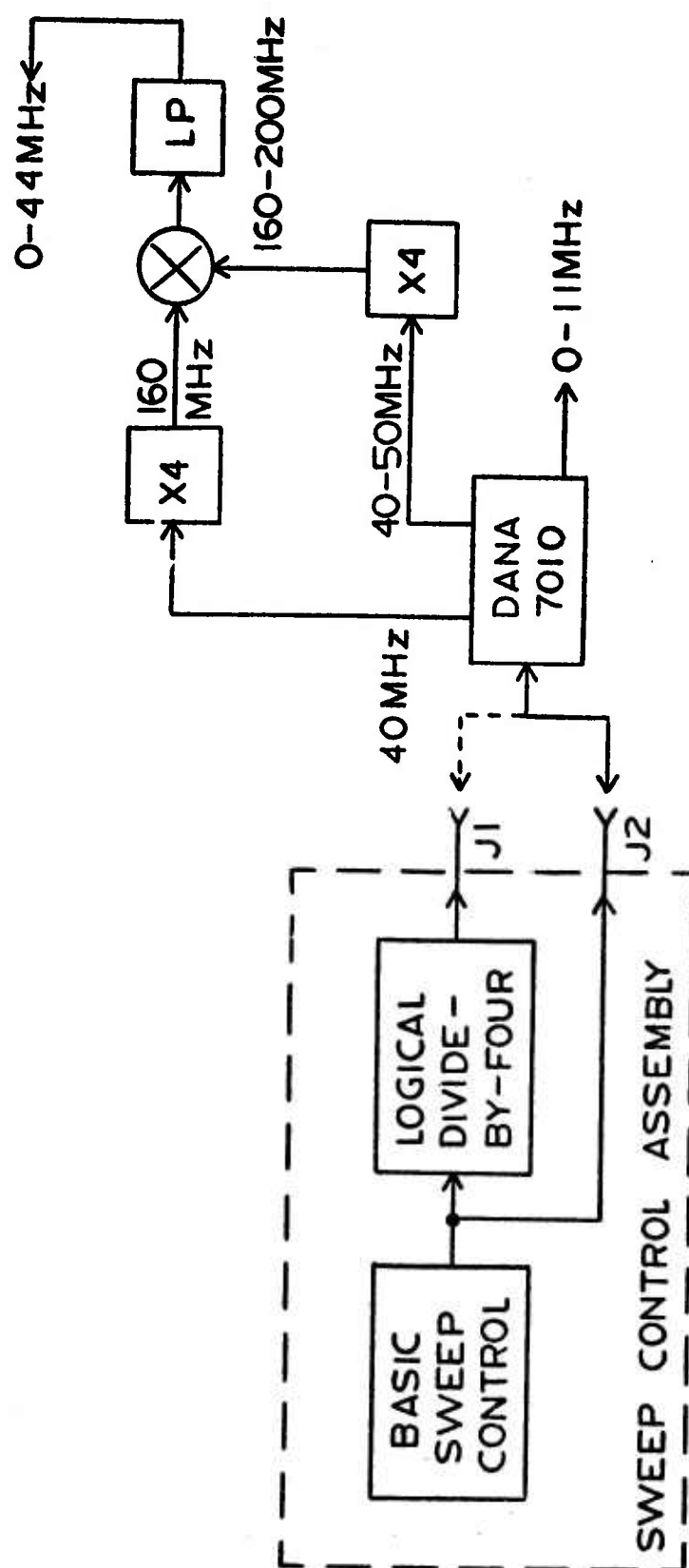
-31-

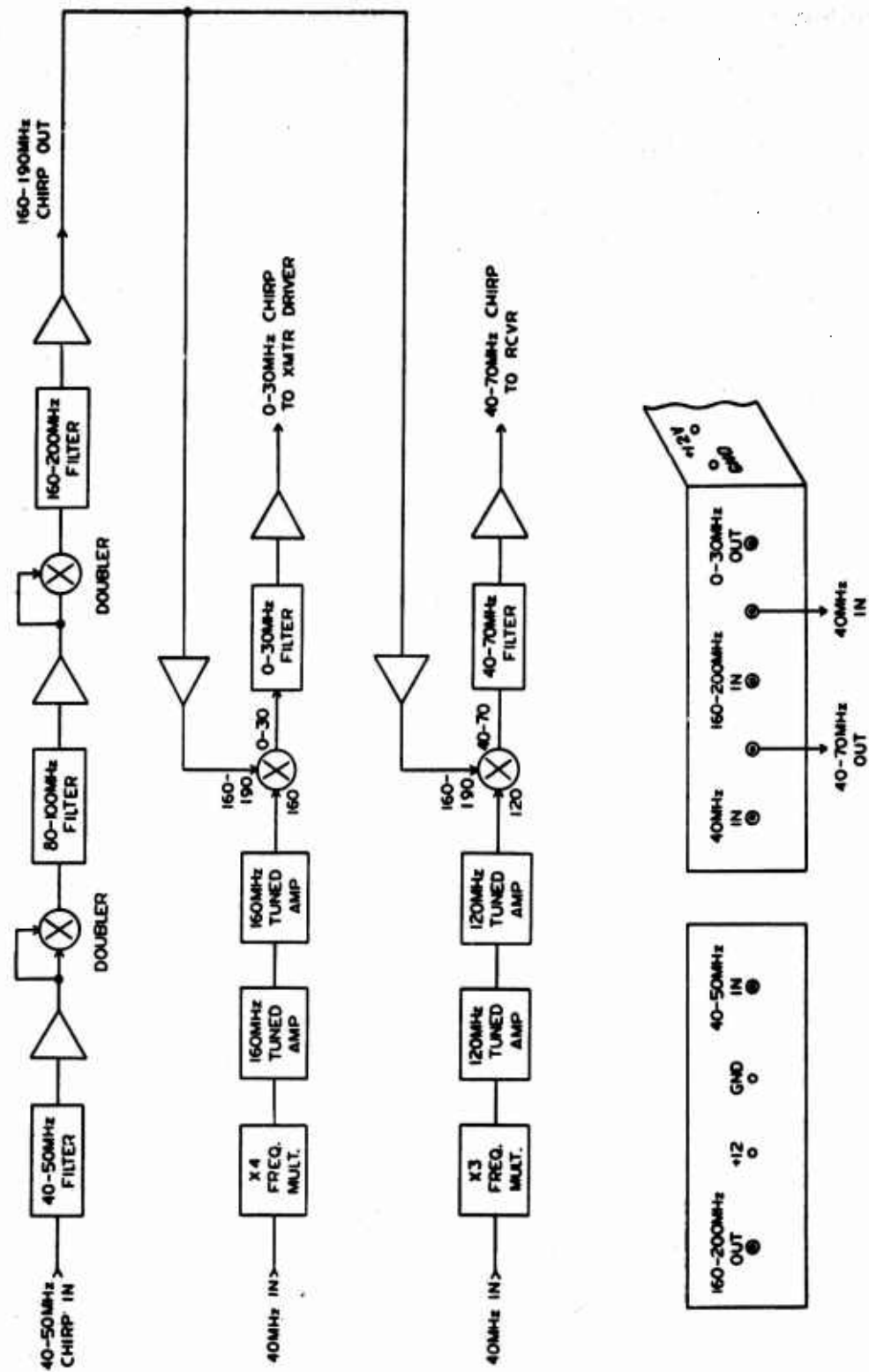FIGURE 2.13   Quadrupling the Frequency Range of the Dana 7010
Frequency Synthesizer

FIGURE 2.14 Vertical Incidence Sounder I Chirp Mult. Block

2.5.2 X4 Multiplier

The top portion of Figure 2.14 depicts the block diagram of the X4 Multiplier. Basically, it consists of a pair of wide-band frequency doublers with bandpass filters, tuned to multiply any frequency in the 40-50 MHz range by four. For this application, the actual used output frequency range is 162 to 190 MHz.

The 40-50 MHz output of the synthesizer is fed through a 40-50 MHz bandpass filter to reduce an undesired out-of-band signals. It is then amplified by about 30 db with a wideband, untuned amplifier and fed to two ports of a broadband balanced mixer. In this configuration, the mixer acts as a frequency doubler, the difference frequency being zero. The sum or doubled frequency, now 80-100 MHz, is passed through an 80-100 MHz bandpass filter to reduce any out-of-band mixing spurs. Again it is amplified and fed to a doubler identical to the previous one. The output signal, now four times the input frequency, is filtered by a 160-190 MHz bandpass filter. A final transistor amplifier provides about 10 db of gain and drives a 50 ohm coax line to the translator sub-assembly.

The remaining portion of Figure 2.14 shows the block diagrams of the receiver and transmitter X4 Translators. The X4 translator multiplies the 40 MHz fixed frequency output of the synthesizer by four and mixes it with the 162-190 MHz multiplier signal. The difference signal, 2-30 MHz, is filtered and amplified to provide the exciter signal for the transmitter. The receiver translator is identical functionally to the

-34-

transmitter translator except that the 40 MHz output of the synthesizer is multiplied by three before mixing it with the 162-190 MHz multiplier signal. The resulting output, 42-70 MHz, is used as the receiver local oscillator.

The 40 MHz output of the synthesizer is coupled to the base of a class C multiplier which has an output tuned to 120 MHz. Following this stage there are two tuned class A amplifiers to provide gain and rejection of unwanted harmonics. The output, which is 120 MHz, is fed to a balanced mixer where it is combined with the 162-190 MHz signal. The difference frequency, 42-70 MHz, is filtered, amplified, and run to a coaxial bulkhead connector where it is available as the receiver first local oscillator. The transmitter translator multiplies the synthesizer 40 MHz output by four with a transistor class-C multiplier. The 160 MHz output is amplified and filtered by two class A stages. fed to a balanced mixer and combined with the 162-200 MHz signal. The difference output is filtered with a 30 MHz low-pass filter, amplified and run to another bulkhead connector where it is available as a transmitter signal source.

The 40 MHz output of the Dana 7010 synthesizer is approximately 175 mv rms, somewhat below the level required to drive the two class C multiplier stages. Buffer amplifiers are provided to bring these levels to one volt rms.

2.6 RECEIVER

The receiver section of the FM/CW vertical incidence sounder consists mainly of a wideband front end, double conversion IF stages, audio amplifier and phase-locked local oscillators (PLLO). The block diagram is shown in Figure 2.15.

The antenna signal from the T/R Switch is run through a balanced mixer which is operated as a switch and gives about 50 db of isolation during the off time. It is followed by a 30 db gain broadband transistor pre-amplifier. The signal is fed through a 2 MHz high pass to a cascade MOS FET amplifier. The attenuation of the filter is approximately 50 db below 1.5 MHz. Following the amplifier is a 30 MHz low-pass filter and another cascade MOS FET amplifier; the filter attenuation is greater than 50 db above 43 MHz. The two filters yield a bandpass from 2 to 30 MHz and are 50 db down at 1.5 and 43 MHz. The second MOS FET amplifier is provided with a manual gain control which varies its gain from + 10 db to - 30 db. This is accomplished by varying the DC bias on the gate of the transistor.

The broadband signal is now fed to a balanced mixer where it is combined with the first receiver local oscillator (l.o.) (42-70 MHz) to provide a 40 MHz IF signal. Before entering the mixer, the 42-70 MHz l.o. signal is fed through a switch similar to that in the antenna circuit and a 42 MHz high-pass filter with a zero at 40 MHz to reduce unwanted

-36-
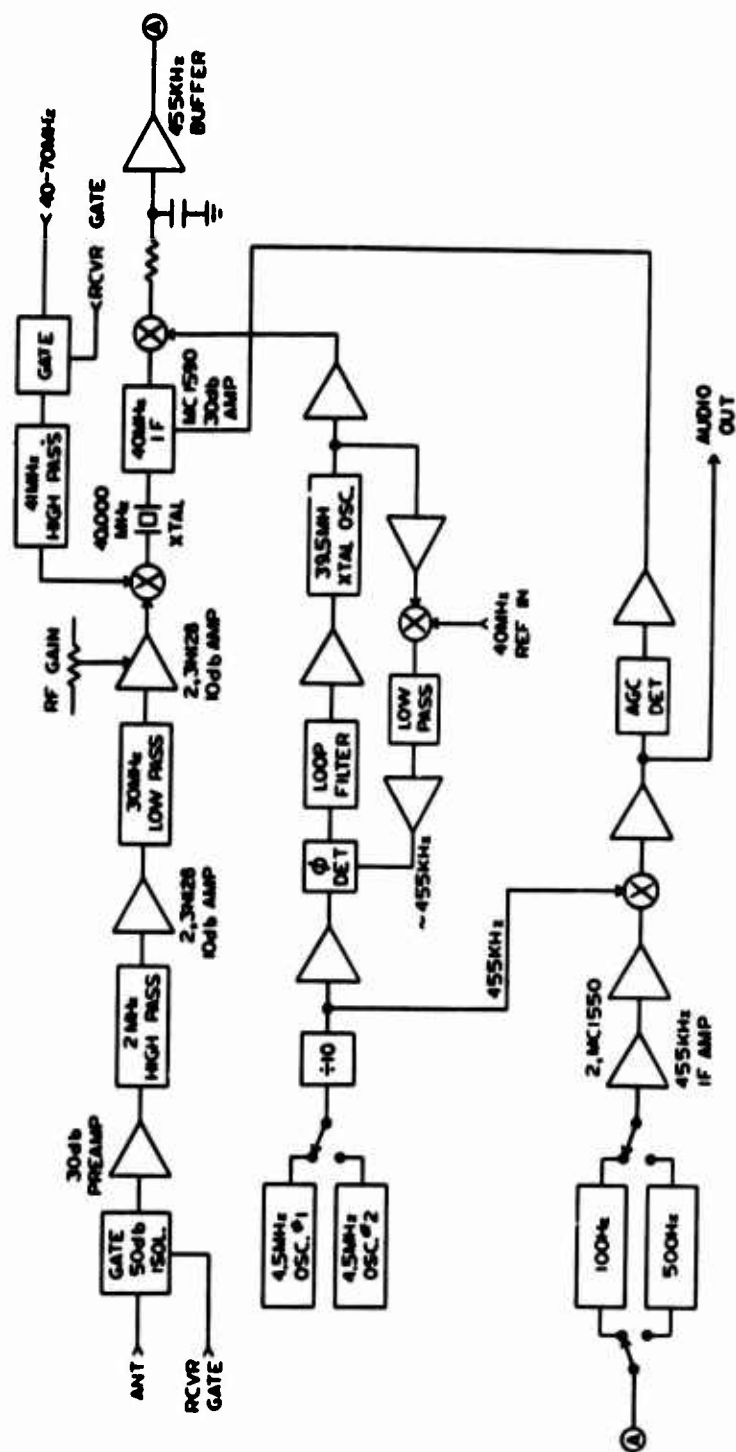
FIGURE 2.15 Vertical Incidence Sounder I RCVR and PLL Block
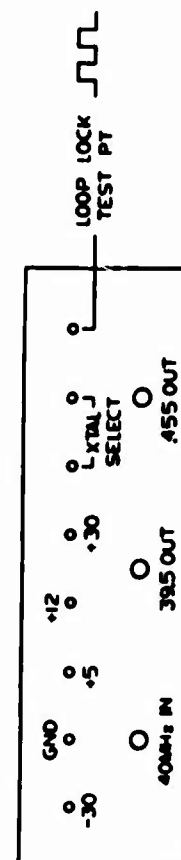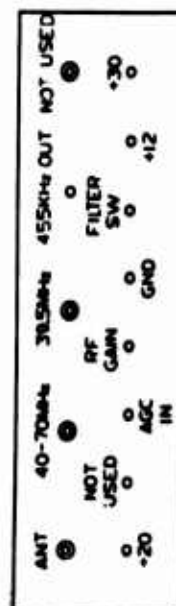
signals that may feed into the IF. As a further precaution, a 40 MHz crystal is incorporated in the IF to attenuate out-of-band signals. A Motorola MC 1590 integrated circuit RF amplifier provides 30 db of IF gain and an AGC range of about 40 db. Following the 40 MHz IF is a balanced mixer that combines the IF signal with the 39.5 MHz signal from the PLLO to produce the 455 kHz second IF frequency. This signal is fed through an R-C low-pass filter to a single stage transistor amplifier that drives second IF bandpass filters. Two filters are provided: one 100 Hz wide and the other 500 Hz wide. They are switched in and out of the signal path with a DPDT relay energized by a front panel switch.

About 60 db of second IF gain is realized by two Motorola MC 1550 RF amplifiers following the filters. The 455 kHz IF signal is now fed to the audio amplifier board where it is mixed with the 455 kHz PLLO signal to provide coherent conversion to a baseband audio output. A Motorola MC 1545 is used as the mixer and is followed by an MC 1456 operational amplifier. The two give a voltage gain of about 60. The MC 1456 stage has a 4700 pf capacitor that can be switched into the feedback network to give a moderate gain boost at 30 Hz. This is used when it is desirable to enhance the returns from the ionospheric E-layer. The E-layer emphasis switch on the front panel controls this function. The output of the MC 1456 is fed to an emitter follower which provides the audio output for the connector on the rear panel. The emitter follower also drives a class C biased transistor that functions as the AGC rectifier. The output is

-38-

fed through an R-C smoothing filter with a long time constant (10 sec). A transistor DC amplifier provides gain to bring the AGC signal level up to the proper voltage (about 7V for full IF gain). A small offset voltage is created by the AGC threshold control on the rear panel to allow some adjustment of the AGC level.

The local oscillator signals for the receiver are generated with a translation-type phaselock loop. The loop is locked to the 40 MHz signal from the Dana synthesizer and includes a 39.5 MHz (nominal) voltage controlled crystal oscillator (VCXO) and a 4.5 MHz fixed crystal oscillator (Figure 2.15). The 39.54508 MHz VCXO output is buffered and mixed with the synthesizer 40.000 000 MHz output to generate a 454.920 kHz signal that is fed through a low-pass filter and amplified. This is compared with the signal generated by the 4.54592 MHz oscillator, divided by 10, in a phase detector. Both signals to the phase detector have been converted to square waves using TTL logic circuitry. The phase detector is a pair of J-K flip flops connected as a set-reset flip flop with complementary outputs fed to an R-C low-pass filter. The DC voltage (phase error voltage) from the low-pass filter is run through an integrating amplifier and applied to voltage variable capacitors in the tank circuit of the 39.5 MHz oscillator to complete the loop.

When operating the receiver with the 500 Hz bandpass IF filter the 4.54740 MHz crystal is switched into the loop. The 39.5 MHz VCXO is pulled approximately 180 Hz up in frequency to keep the loop locked.

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2.7 T/R SWITCH ASSEMBLY

The T/R switch assembly permits the sounder to transmit and
receive on the same antenna. It is capable of passing 10 Watts from the
rf power amplifier to the antenna and yet provides 40 db of isolation of the
receiver from the transmitter output when the receiver is connected to
the antenna (see Figure 2.16) At least this amount of isolation is required
since the transmitter broadband noise floor is at least 58 db above kTB
at the output (equivalent to 12 db noise figure followed by 46 db gain).

2.7.1 Circuit Description

As Figure 2.16 indicates, the T/R Switch assembly is comprised
of two identical SP DT switches. Both are controlled by the same T/R
control signal from the PRF board in the receiver assembly. The T/R
control is a TTL output that is converted into a pair of driver outputs
A and B that alternate between levels of plus and minus 25 volts providing
a 50 volt difference between these outputs.

Whether A is up and B is down or vice versa, 500 milliamps flow
between driver outputs A and B. The current is limited by a 100Ω
resistor in the RF switch portion. In the "Normally Closed" state,
A is high and B is low. Current flows into the center tap of the T2, then
divides equally to flow through D3 and D4, and finally out of the T5 center
tap back into B. Thus an RF path from the "Common" output to the "NC"
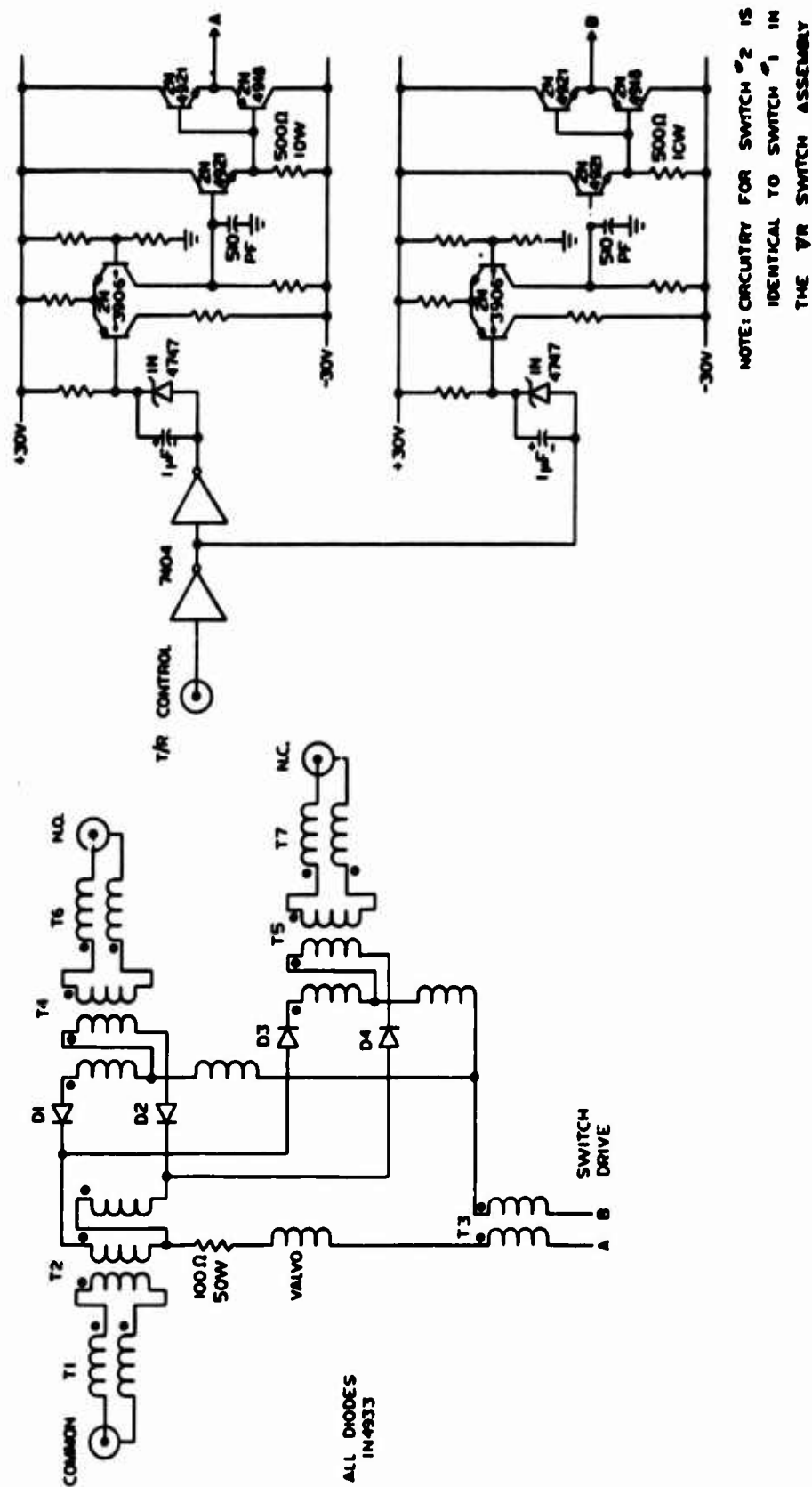input is completed.

FIGURE 2.16 Vertical Incidence Sounder, T/R Switch Assembly, Switch #1

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If "Common" is terminated with 50 ohms T2 steps up two-to-one providing a 200 ohm termination across D3 and D4. T5 steps down again presenting "NC" with a 50 ohm termination. Thus if "NC" were fed 10 Watts of RF the peak RF current in D3 or D4 is 316 milliamps. Since the quiescent current in each is only 250 milliamps, the peak reverse RF flow is partially dependent on the stored charge in D3 and D4.

RF isolation at the "Normally Open" receptacle is limited to the capacitance of D1 and D2 in series with a reverse bias of 50 volts. A lower bias voltage would result in higher capacitances and less isolation.

3.0 AUXILIARY DRIVER UNIT

3.1 AUXILIARY DRIVER UNIT FOR MODIFIED HP 5100 FREQUENCY SYNTHESIZER

Relatively extensive maintenance has been found to be required on the modified Hewlett-Packard Model 5100 driver unit which supplies the 3.0-3.9 and 30-39 MHz fixed frequency reference signals to the synthesizer. In order to achieve coherent operation, the phase and amplitude of the 3.0-3.9 MHz reference signals must be closely controlled. In practice, the phase shifts were found to be somewhat temperature dependent and that while the phase errors could be brought within the original design specifications, the range of adjustment and the difficulty of making said adjustment precluded reliable coherent operation. Consequently, auxiliary frequency sources were designed to replace the 3.0-3.9 MHz reference signals of the HP 5110 driver units for three of the FM/CW synthesizers.

The FM/CW Auxiliary Driver provides 10 reference frequencies spaced at 100 kHz intervals between 3.0 and 3.9 MHz which are phase locked to an external 100 kHz clock. In practice, this clock is obtained from the FM/CW Synthesizer Control Unit. The zero crossing points of two signals spaced by multiples of 100 kHz coincide at least once every 10 μsec; the phase relationships between the 10 reference frequencies are adjusted such that a coincident zero crossing occurs and the use of the synthesizer 100 kHz clock permits a definite relationship to be

established and maintained between the coincident zero crossing of the reference frequency signals and the matrix switching commands generated by the Control Unit. A photograph (front view) of the unit is shown in Figure 3. 1 and a rear view with cover removed in Figure 3. 2. Coarse adjustment of the temporal position of the zero crossing is provided in 0.1μ sec increments from 0 to 9.5μ sec by a front panel thumbwheel switch with fine phasing accomplished by adjustment of a control on each individual reference oscillator. Ten push-button indicator lamps on the front panel serve to indicate loss of phase lock; depressing the button causes the loop to loose lock and the indicator lamp illuminates and subsequently extinguishes when lock is reacquired, serving to test both the indicator lamps and each phase-locked loop.

The unit consists of four basic sections:

    a)   logic control card

    b)   oscillators and lamp driver

    c)   temperature regulator

    d)   power supply

An overall block diagram is shown as Figure 3. 3.

3.1.1 <u>Oscillators and Lamp Driver</u>

The oscillators unit consists of eleven phase-locked crystal controlled oscillators (3.0 to 3.9 MHz in 100 kHz steps and 10 MHz) each on an individual printed circuit card and a lamp driver card and located in a single assembly. The 3.0-3.9 MHz oscillators are basically crystal
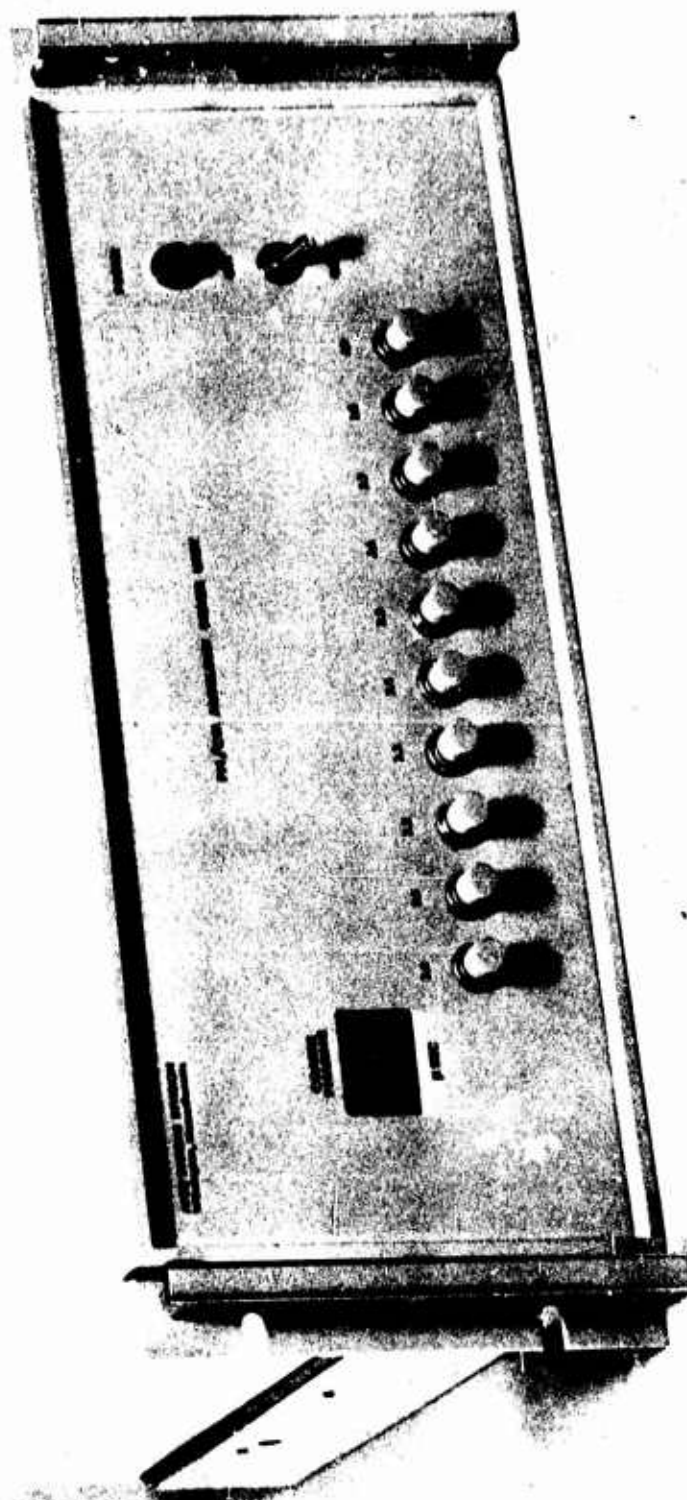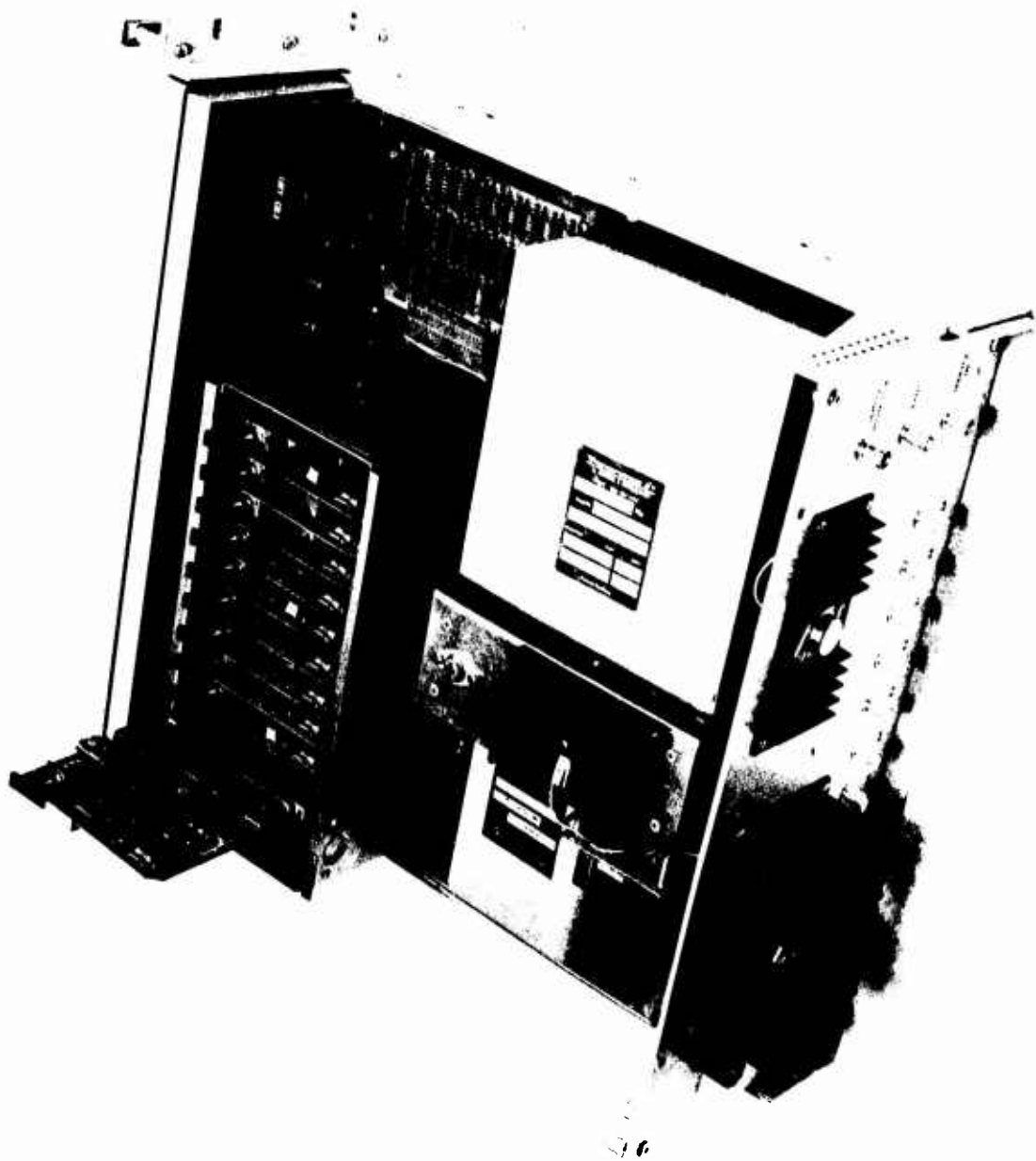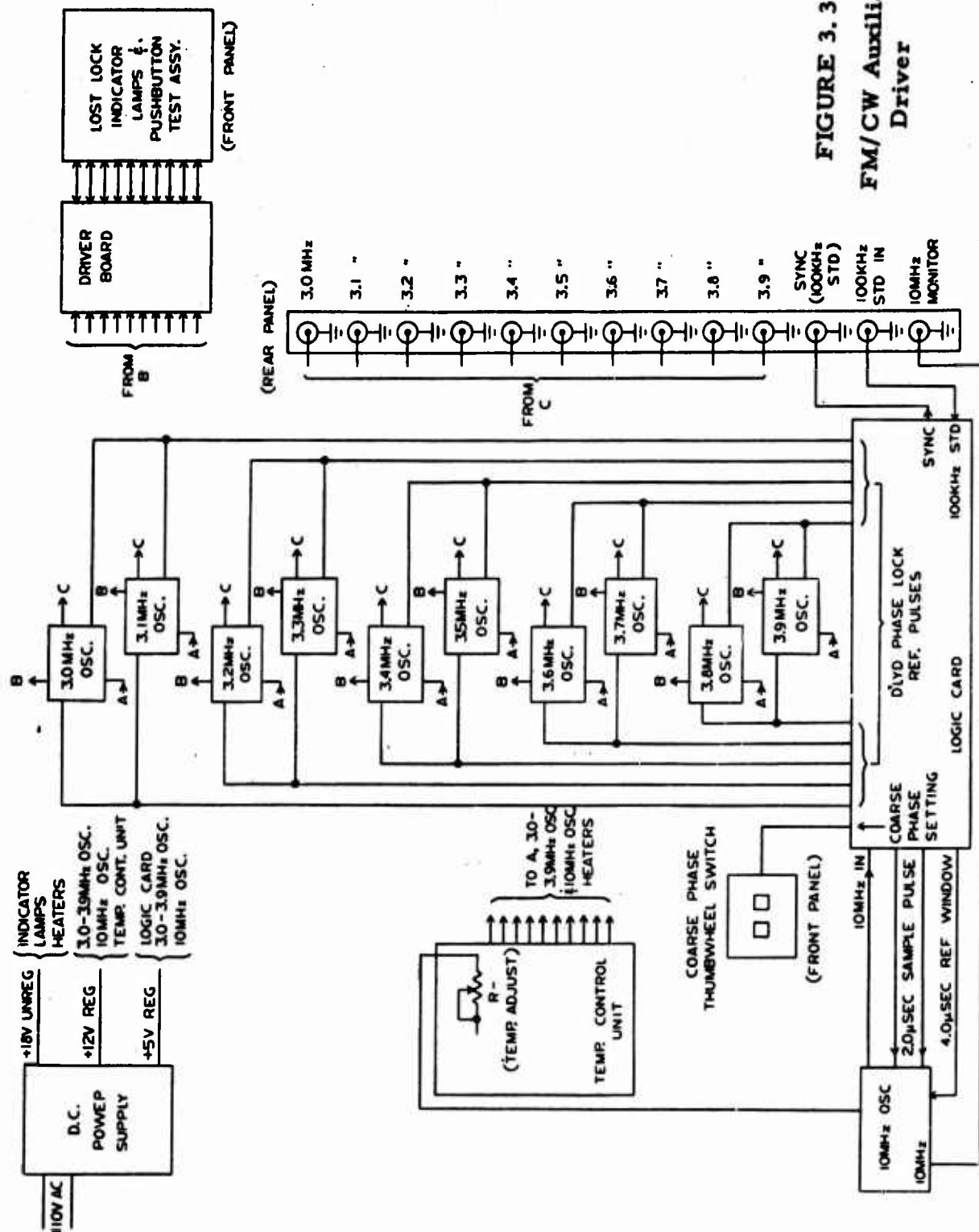
-44-

FIGURE 3.1

FIGURE 3.2

FIGURE 3.3
FM/CW Auxiliary Driver

controlled Butler oscillators phase locked to a 100 kHz reference. Phase lock is accomplished by sampling in a 0.4μsec window at the reference rate. Any unbalance is detected, amplified, and filtered and applied to voltage variable capacitors located in the tuned circuit. The temporal position of the sampling window is adjustable over 9.4μsec in 0.1μsec increments with respect to the 100 kHz reference clock by the coarse phasing thumbwheel switch located on the front panel. Since the sampling window is common to all the oscillator units, the position of the coincident zero crossings become adjustable over 9.4μsec with respect to the clock.

The schematic diagram for a typical oscillator module is shown in Figure 3.4. An independent fine phase adjustment is provided by R-2. The phase-locked signal is low-pass filtered and is matched to the 50Ω coaxial cable output by an emitter follower. Each oscillator output is brought to a rear panel BNC and the connectors are configured to permit the use of the existing cable assembly previously used to connect to the Hewlett-Packard driver unit.

The 10 MHz oscillator is a crystal controlled Butler type oscillator which is phase locked to the 100 kHz clock. This 10 MHz signal is supplied to the logic control card to derive the 0.1μsec coarse phasing steps and is available at the rear panel as a test point.

The lamp driver board consists of 10 Schmitt triggers, each associated with an oscillator unit. When actuated, it turns on a lamp driver transistor illuminating the front panel light designating the oscillator unit which has lost lock.

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FIGURE 3.4

Auxiliary Driver Unit
3.0-3.0 MHz Oscillators
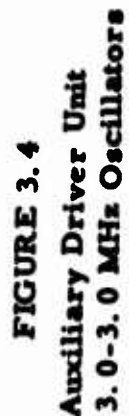
3.1.2 Logic Control Card

The basic function of the logic board is to condition the externally supplied 100 kHz signal so that it may be utilized to phase lock the 3.0-3.9 MHz and 10 MHz oscillators. In addition, this assembly generates the common 4μ sec window for shifting the zero crossing point of the phase locked oscillators in 0.1μ sec increments. This resolution results from counting down the 10 MHz oscillator with control by the coarse positioning thumbwheel switch on the front panel. The block diagram is shown in Figure 3.5.

The external 100 kHz signal is bandpass filtered to minimize external noise, squared up by two buffer amplifiers and simultaneously fed to a buffered sync output on the rear panel and a pulse shaping network. The shaped pulse triggers a monostable multivibrator generating a 4μ sec window utilized to phase lock the 10 MHz oscillator; the pulse also resets a flip flop, resetting a divide-by-eight counter and enabling the coarse phasing count-down circuit. At the conclusion of the preset count down, the divide-by-eight circuit is enabled, generating two concurrent 2μ sec phase locking sample gates which are supplied to the 3.0 - 3.9 MHz oscillator boards through buffers. The 10 MHz oscillator signal is fed to the logic board where it is buffered and fed to the count-down circuits.

3.1.3 Temperature Regulator

The temperature regulator is of the proportional control type, chosen to prevent thermal transients. Each of the 3.0-3.9 MHz
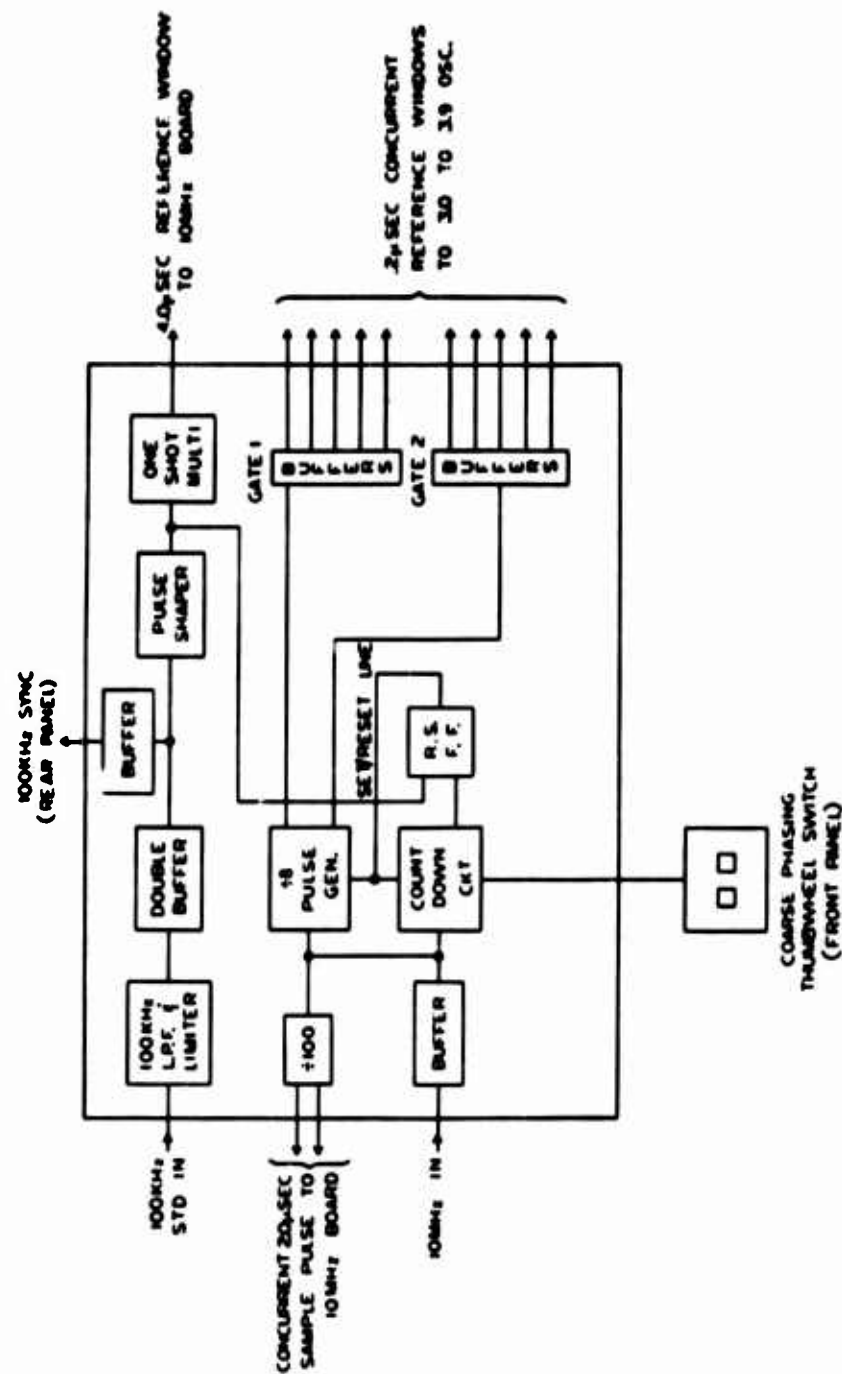
FIGURE 3.5   Auxiliary Driver Unit Logic Board

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oscillator cards has a separate resistive heater element, but temperature sensing is performed only on the 3.5 MHz card. The operating temperature has been set at 37°C. Control of the temperature can be accomplished by a potentiometer adjustment, but change of the set point is not recommended.

3.1.4 Power Supply

The power supply is self contained and operates from prime power of 115 VAC, 60 Hz. The DC voltages are 18 volts unregulated, 12 volts regulated and unregulated, and 5 volts regulated. The indicator lamps and heaters utilize 18 volts unregulated. The 12 volt regulated supply is derived from the 18 volt supply through a MC1469 integrated circuit regulator while the 5 volt regulated is derived from the 12 volt unregulated supply through a LM309 regulator mounted on the rear panel.

3.2 PHASE BOARDS FOR MODIFIED HP 5100 FREQUENCY SYNTHE-SIZER

Coherent operation of the Hewlett-Packard Model 5100 direct digital frequency synthesizer requires the development of up to five separate phase shifted signals derived from each of the ten 3.0-3.9 MHz fixed frequency phase stable signals produced by the Hewlett-Packard Model 5110 driver unit. The approach initially taken in the development of the prototype (SN001) FM/CW generator involved the use of tapped delay lines. Evaluation of this concept revealed that it was not entirely satisfactory in that insufficient fine control of the amplitude and phase

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existed and that cross-coupling between the various phases occurred as a result of loading changes when the matrix switches were energized; additionally impulsive modulation associated with switch unbalance could couple through to the rf output.

The electromechanical delay lines were replaced by all-pass filter networks constructed of lumped constant elements and adjusted to yield the appropriate relative phase delays at each of the reference frequencies. Each phase source was buffered by an emitter follower which served to isolate the phases from feed through of switching transients and loading changes, and which reduced the amplitude transient by providing a lower source impedance. Control of the amplitude of each reference signal is provided by a multi-turn potentiometer. Each phase can be monitored separately at the emitter follower output through a 0.1 μ farad capacitor without removing the phasing board from the unit.

At the time that these changes were made, the cables carrying the switching signals from the sweep control unit to the matrix switch driver board located within the synthesizer occasionally broke. Cable clamps were added to prevent bending stress and tension from being applied to the soldered connections.

APPENDIX A

A-1

SINGLE ANTENNA VERTICAL-INCIDENCE MODULATION PHILOSOPHY; A HEURISTIC EXPLANATION

Ordinarily, the linear FM/CW waveform has been utilized for ionospheric sounding as a unity duty factor waveform. As such, after decommutation, the return from a single reflecting surface was characterized as a single fixed frequency, ultimately converted to baseband and detected by spectrum analysis. If the desired signal is characterized as $f_i(t) = A_i \sin \omega_i t$ where the properties of A_i and ω_i are slowly varying functions of times. A random noise background, consisting of either external (atmospheric) or receiver generated is presumed to exist and to have properties which may be treated as "random". We can assume that it possesses a power spectral density equivalent to Vn_{rms} per Hz of detection bandwidth. Thus, the achieved signal to noise ratio is

$$\frac{S}{N} = \frac{0.707 \, A_i}{Vn_{rms}} \tag{A-1}$$

When the single-antenna sounder concept is utilized, the duty factor is no longer unity, and the selection of the receive duty factor is a design choice. One factor which influences the choice is the achieved signal-to-noise ratio. We show in Figure A-1 the transmit and receive time gates for 50, 25, and 12.5 percent receive duty cycles, the transmit duty cycles being 50, 75, and 87.5 percent, respectively. The short time interval which, in practice, separates the transmit and receive modes to avoid complications due to switching transients is neglected. The transmitter

off period results in zeros in the range visibility function, whose amplitude is computed as the cross-correlation of the transmit and receive envelope functions, and is also shown in Figure A-1. The average value of the visibility function β_{12} is seen to be linearly dependent on the transmit duty cycle, since the peak transmitted power is constant. Hence, the average value of the desired return is proportional to the transmit duty cycle. (The zeros in the range visibility function are eliminated by the selection of a pseudo-random prf in the practical realization of this system.)

When the received signal is modulated by the switching waveform, the result, after decommutation, is the sine wave $f_1(t)$ now a spectrum with sin x/x characteristics; spectral lines are found at frequencies that are a function of the fundamental and harmonics of the prf, and the envelope function is nominally scaled as the inverse of the receiver on time. The prf is chosen such that the first sidebands fall outside the last IF filter and are attenuated such that the sidebands do not fold into the spectrum analyzer bandwidth when the decommutated signal is translated to baseband.

The amplitude of the desired spectral component is reduced by the duty factor such that

$$F_1(t) = A_1 \left(\frac{t_0}{T}\right) \sin \omega_1 t \qquad (A-2)$$

where t_0 is the receiver on time

T is the pulse repetition time

The noise background, which is broadband in nature, results in a variation with duty cycle given by

$$\mathcal{V}n_{rms} = Vn_{rms}\left(\frac{t_o}{T}\right)^{1/2} \qquad \text{(A-3)}$$

Consequently, combining equations A-2, A-3, and the linear dependence of A_l on the average power in the form of A-1, we find the relationship of the signal-to-noise ratio with duty cycle for the single-antenna sounder to be

$$\frac{S}{N} = \frac{0.707\, A_l \left(\frac{t_o}{T}\right)}{Vn_{rms}\left(\frac{t_o}{T}\right)^{1/2}} \quad \left(1 - \frac{t_o}{T}\right)$$

$$\text{(A-4)}$$

$$= \frac{0.707\, A_l}{Vn_{rms}} \left(\frac{t_o}{T}\right)^{1/2} \left(1 - \frac{t_o}{T}\right)$$

Hence, the achieved signal-to-noise ratio is proportional to

$$Q = \left(\frac{t_o}{T}\right)^{1/2} \left(1 - \frac{t_o}{T}\right) \qquad \text{(A-5)}$$

which is computed for several duty cycles and presented in Table A-1.

Table A-1

t_o	0.75	0.5	0.25	0.125
Q	.2165	.3536	.3750	.3094

From this result one can infer that a receive duty factor of the order of 0.25 is the optimum choice, although the maximum is relatively broad. Ordinarily, the prf is wobulated in a pseudo-random manner to fill in the range visibility zeros. Since the width, in time delay of the visibility zeros decreases with decreasing receive duty cycle, the percentage variation of prf required to achieve a relatively uniform visibility function becomes smaller as the receive duty cycle is reduced.

$$\phi_{12}(\tau) = \frac{T}{t_0} \int_0^T f_1(t) \, f_2(t + \tau) \, dt$$
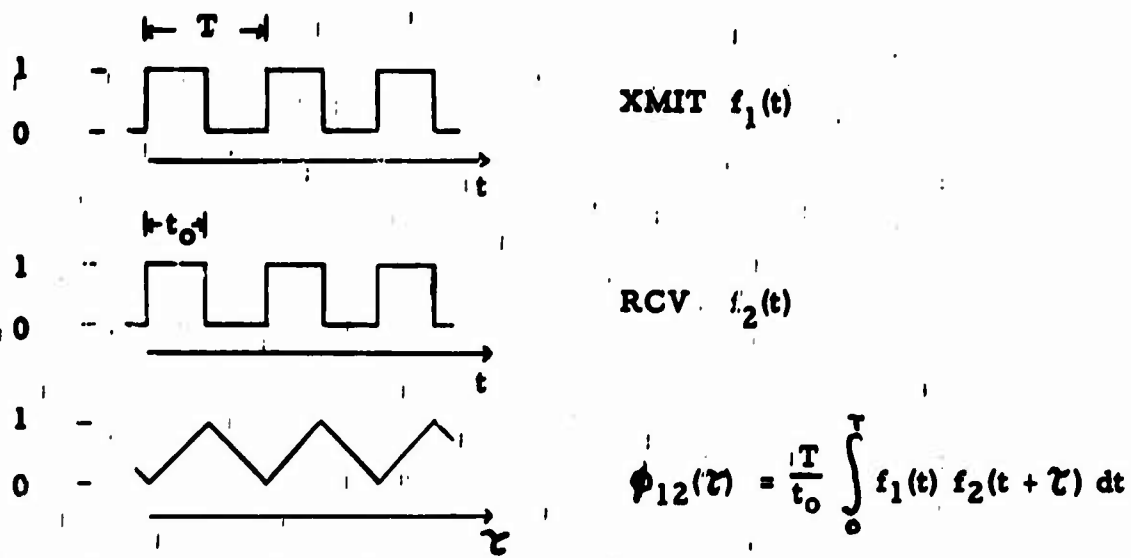
a) 50% Receive Duty Cycle
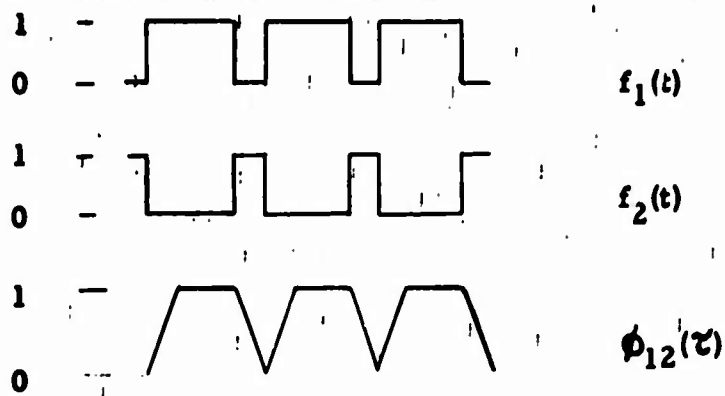
b) 25% Receive Duty Cycle
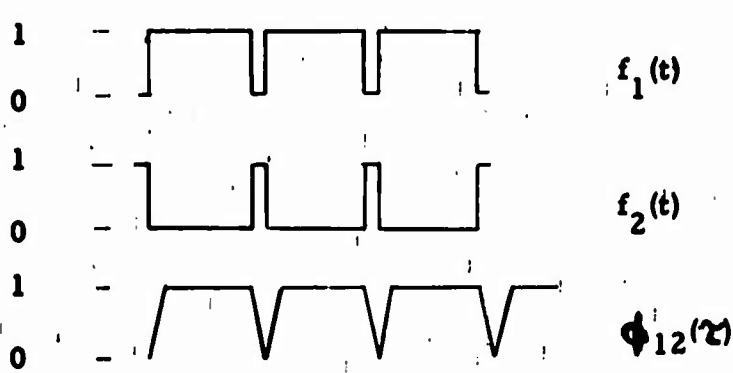
c) 12.5% Receive Duty Cycle

FIGURE A-1. Deriving the Normalized Visibility Function, $\phi_{12}(\tau)$
Where τ is the Round-Trip Delay